4-Channel Automotive Smart Half-Bridge Gate Drivers with Wide Common Mode Inline Current Sense Amplifiers

GENERAL DESCRIPTION

The SiLM9714-AQ is highly integrated 4-Channel gate drivers intended for driving multiple motors or loads. It integrates four half-bridge gate drivers, driver power supplies, current shunt amplifiers, and protection monitors reducing total system complexity, size and cost.

A smart gate drive architecture manages dead time to prevent shoot-through, controls slew rate to decrease electromagnetic interference (EMI), and optimizes propagation delay for optimal performance.

Input modes are provided for independent half- bridge or H-bridge control. Four PWM inputs can be multiplexed between the different drivers in combination with SPI control.

Wide common mode shunt amplifiers provide inline current sensing to continuously measure motor current even during recirculating windows. The amplifier can be used in low-side or high-side sense configurations if inline sensing is not required.

The devices provide an array of protection features to ensure robust system operation. These include under and overvoltage monitors, V_{DS} overcurrent and V_{GS} gate fault monitors for the external MOSFETs, offline open load and short circuit diagnostics, and internal thermal warning and shutdown protection.

APPLICATIONS

- Automotive brushed DC motors
- Power seat modules
- Power trunk and lift gate
- Door module
- Body control modules
- Power sunroof
- Transmission and engine control modules

FEATURES

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- 4-Channel half-bridge gate drivers
  - 4.9V to 37V (40V abs. max) operating range
  - 4 PWM inputs with output mapping
  - Tripler charge pump for 100% PWM
  - Half-bridge, H-bridge and SPI control modes
- Smart multi-stage gate drive architecture
  - Adjustable slew rate control
  - Adaptive propagation delay control
  - 50µA to 62mA peak source current output
  - 50µA to 62mA peak sink current output
  - Integrated dead-time handshaking
- Two wide common mode current shunt amplifiers
  - Supports inline, high-side or low-side
  - Adjustable gain settings (10, 20, 40, 80 V/V)
- SPI: Detailed configuration and diagnostics
- Integrated protection features
  - Dedicated driver disable pin (DRVOFF)
  - Low I_Q, sleep mode motor braking (BRAKE)
  - Supply and regulator voltage monitors
  - MOSFET V_{DS} overcurrent monitors
  - MOSFET V_{GS} gate fault monitors
  - Charge pump for reverse polarity MOSFET
  - Offline open load and short circuit diagnostics
  - Device thermal warning and shutdown
  - Window watchdog timer.
  - Fault condition interrupt pin (nFAULT)
  - 3.3 V and 5 V logic compatible
- Package：QFN40 or QFN56

DEVICE BLOCK TABLE

Table 1.SiLM9714-AQ Function Blolck Table

Feature	Configuration
PWM Input Mode	4 Modes
Gate Drive Output Current (I_{DRIVE})	16 Settings
DeadTime	Handshake + 3 Fixed Settings
V_{DS} Comparator Threshold	16 Settings
V_{DS} and V_{GS} Blanking Time (t_{DRIVE})	8 Settings
V_{DS} Deglitch Time	4 Settings
V_{GS} Deglitch Time	Fixed, 2 µs
V_{DS} Fault Response	4 Modes
V_{GS} Fault Response	4 Modes
AmplifierGain	4 Settings
Amplifier Blanking Time	8 Settings
Amplifier Reference Voltage	2 Settings
V_{PVDD} Undervoltage Fault Response	2 Modes
V_{PVDD} Overvoltage Fault Response	4 Modes
V_{VCP} Undervoltage Fault Response	2 Modes
V_{VCP} Undervoltage Threshold	2 Settings
Offline Open Load Diagnostic	Available
Offline Short Circuit Diagnostic	Available
WatchdogTimer	Available
Multi-Function DRVOFF/nFLT Pin	Configurable DRVOFF or nFLT

ORDERING INFORMATION

Order Part No.	Package	QTY
SiLM9714SET-AQ	QFN40, 6x6 mm, Pb-Free	2500/Reel
SiLM9714SEV-AQ	QFN56, 8x8 mm, Pb-Free	2000/Reel

40-PIN PACKAGE CONFIGURATION

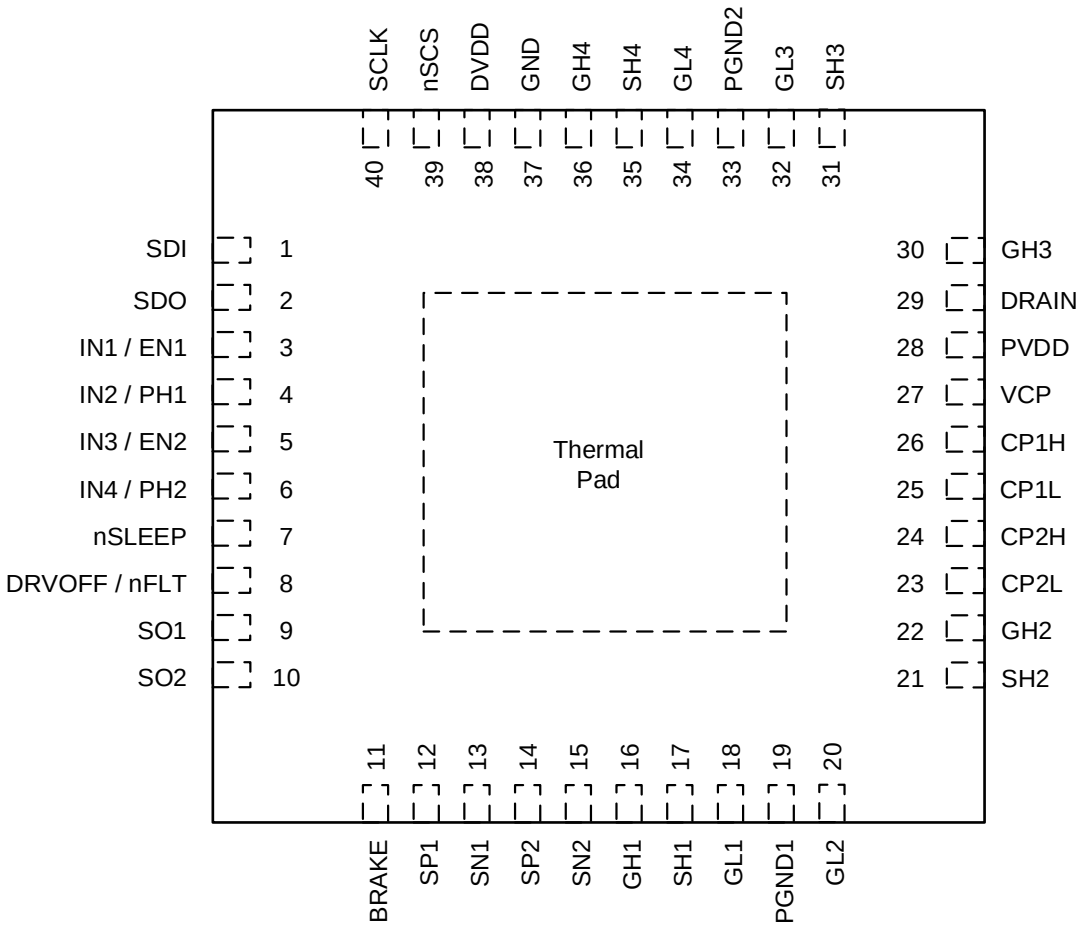


Figure 1. SiLM9714-AQ QFN40 Package (Top View)

40-PIN PACKAGE PIN DESCRIPTION

No.	Pin Name	I/O	Type	Description
1	SDI	I	Digital	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pulldown resistor.
2	SDO	O	Digital	Serial data output. Data is shifted out on the rising edge of the SCLK pin. Push-pull output.
3	IN1/EN1	I	Digital	Half-bridge and H-bridge control input. Internal pulldown.
4	IN2/PH1	I	Digital	
5	IN3/EN2	I	Digital	
6	IN4/PH2	I	Digital	
7	nSLEEP	I	Digital	Device enable pin. Logic low to shutdown the device and enter sleep mode. Internal pulldown resistor.
8	DRVOFF/nFLT	I/O	Digital	Multi-function pin for either driver shutdown input or fault indicator output. Internal pulldown resistor.
9	SO1	O	Analog	Shunt amplifier output.
10	SO2	O	Analog	Shunt amplifier output.
11	BRAKE	I	Digital	Powered off braking pin. Logic high to enable low-side gate drivers while in low-power sleep mode. Internal pulldown resistor.
12	SP1	I	Analog	Amplifier positive input. Connect to positive terminal of the shunt resistor.
13	SN1	I	Analog	Amplifier negative input. Connect to negative terminal of the shunt resistor.
14	SP2	I	Analog	Amplifier positive input. Connect to positive terminal of the shunt resistor.
15	SN2	I	Analog	Amplifier negative input. Connect to negative terminal of the shunt resistor.
16	GH1	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
17	SH1	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
18	GL1	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
19	PGND1	I	Analog	Low-side MOSFET gate drive 1-2 sense and power return. Connect to system ground close to the device and half-bridge 1-2.
20	GL2	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
21	SH2	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.

No.	Pin Name	I/O	Type	Description
22	GH2	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
23	CP2L	I/O	Power	Charge pump switching node. Connect a 100-nF, PVDD-rated ceramic capacitor between the CP2H and CP2L pins.
24	CP2H	I/O	Power	
25	CP1L	I/O	Power	Charge pump switching node. Connect a 100-nF, PVDD-rated ceramic capacitor between the CP1H and CP1L pins.
26	CP1H	I/O	Power	
27	VCP	I/O	Power	Charge pump output. Connect a 1-µF, 16-V ceramic capacitor between the VCP and PVDD pins.
28	PVDD	I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1-µF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10-µF between PVDD and GND pins.
29	DRAIN	I	Analog	Bridge MOSFET drain voltage sense pin. Connect to common point of the high-side MOSFET drains.
30	GH3	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
31	SH3	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
32	GL3	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
33	PGND2	I	Analog	Low-side MOSFET gate drive 3-4 sense and power return. Connect to system ground close to the device and half-bridge 3-4.
34	GL4	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
35	SH4	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
36	GH4	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
37	GND	I/O	Ground	Device ground. Connect to system ground.
38	DVDD	I	Power	Device logic and digital output power supply input. External voltage reference and power supply for current sense amplifiers. Recommended to connect a 1.0-µF, 6.3-V ceramic capacitor between the DVDD and GND pins.
39	nSCS	I	Digital	Serial chip select. A logic low on this pin enables serial interface communication. Internal pullup resistor.
40	SCLK	I	Digital	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pulldown resistor.

56-PIN PACKAGE CONFIGURATION

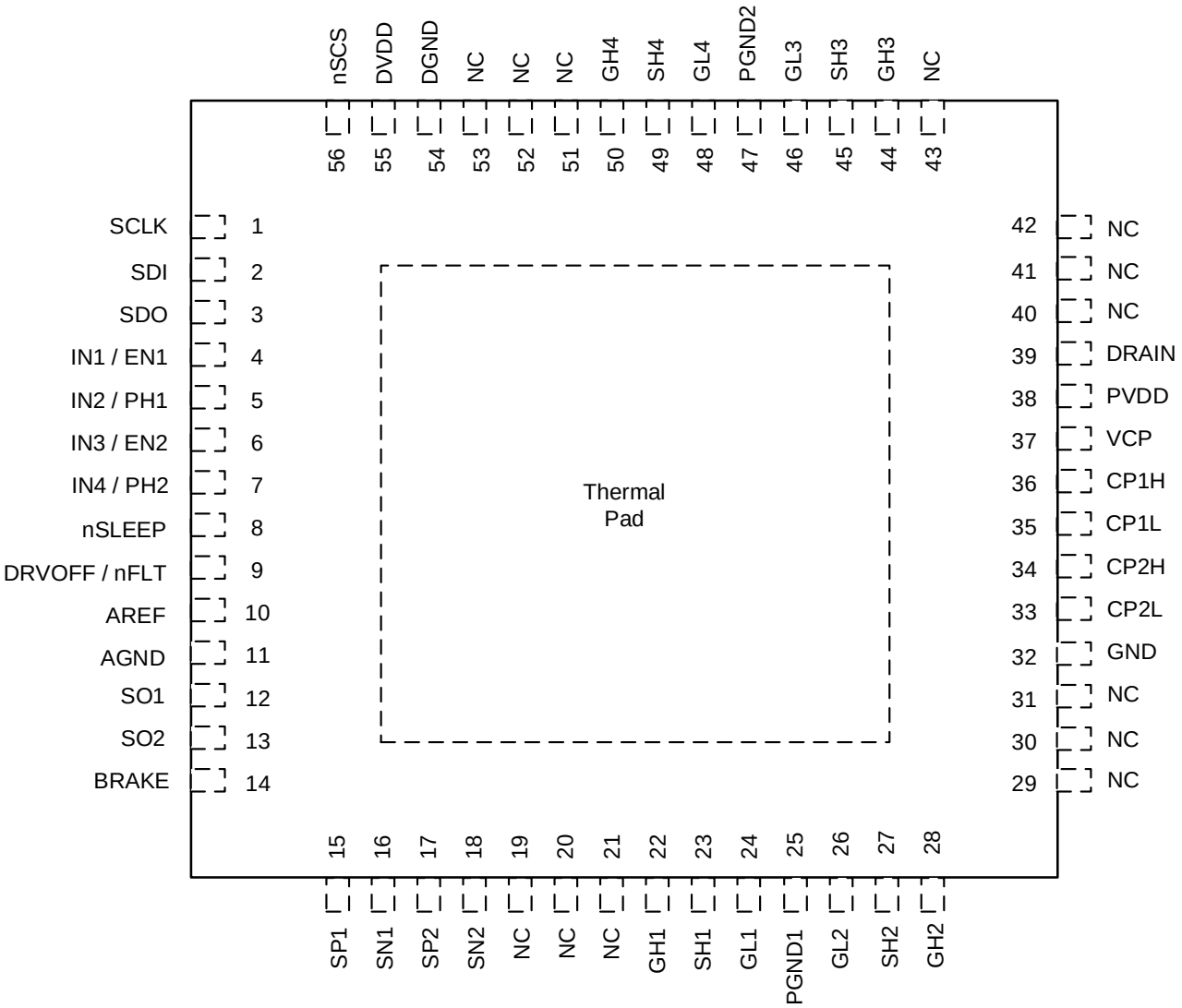


Figure 2. SiLM9714-AQ QFN56 Package (Top View)

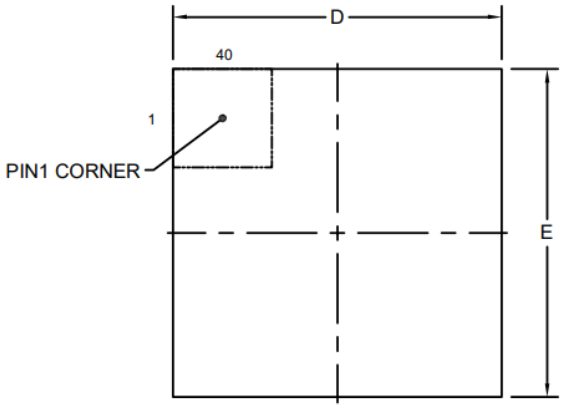
56-PIN PACKAGE PIN DESCRIPTION

No.	Pin Name	I/O	Type	Description
1	SCLK	I	Digital	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pulldown resistor.
2	SDI	I	Digital	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pulldown resistor.
3	SDO	O	Digital	Serial data output. Data is shifted out on the rising edge of the SCLK pin. Push-pull output.
4	IN1/EN1	I	Digital	Half-bridge and H-bridge control input. Internal pulldown.
5	IN2/PH1	I	Digital	
6	IN3/EN2	I	Digital	
7	IN4/PH2	I	Digital	
8	nSLEEP	I	Digital	Device enable pin. Logic low to shutdown the device and enter sleep mode. Internal pulldown resistor.
9	DRVOFF/nFLT	I/O	Digital	Multi-function pin for either driver shutdown input or fault indicator output. Internal pulldown resistor.
10	AREF	I	Power	External voltage reference and power supply for current sense amplifiers. Recommended to connect a 0.1-μF, 6.3-V ceramic capacitor between the AREF and AGND pins.
11	AGND	I/O	Ground	Device ground. Connect to system ground.
12	SO1	O	Analog	Shunt amplifier output.
13	SO2	O	Analog	Shunt amplifier output.
14	BRAKE	I	Digital	Powered off braking pin. Logic high to enable low-side gate drivers while in low-power sleep mode. Internal pulldown resistor.
15	SP1	I	Analog	Amplifier positive input. Connect to positive terminal of the shunt resistor.
16	SN1	I	Analog	Amplifier negative input. Connect to negative terminal of the shunt resistor.
17	SP2	I	Analog	Amplifier positive input. Connect to positive terminal of the shunt resistor.
18	SN2	I	Analog	Amplifier negative input. Connect to negative terminal of the shunt resistor.
19	NC	—	—	No connection.
20	NC	—	—	No connection.
21	NC	—	—	No connection.

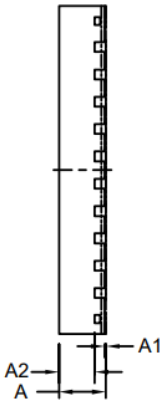
No.	Pin Name	I/O	Type	Description
22	GH1	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
23	SH1	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
24	GL1	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
25	PGND1	I	Analog	Low-side MOSFET gate drive 1-2 sense and power return. Connect to system ground close to the device and half-bridge 1-2.
26	GL2	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
27	SH2	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
28	GH2	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
29	NC	—	—	No connection.
30	NC	—	—	No connection.
31	NC	—	—	No connection.
32	GND	I/O	Ground	Device ground. Connect to system ground.
33	CP2L	I/O	Power	Charge pump switching node. Connect a 100-nF, PVDD-rated ceramic capacitor between the CP2H and CP2L pins.
34	CP2H	I/O	Power	
35	CP1L	I/O	Power	Charge pump switching node. Connect a 100-nF, PVDD-rated ceramic capacitor between the CP1H and CP1L pins.
36	CP1H	I/O	Power	
37	VCP	I/O	Power	Charge pump output. Connect a 1-µF, 16-V ceramic capacitor between the VCP and PVDD pins.
38	PVDD	I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1-µF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10-µF between PVDD and GND pins.
39	DRAIN	I	Analog	Bridge MOSFET drain voltage sense pin. Connect to common point of the high-side MOSFET drains.
40	NC	—	—	No connection.
41	NC	—	—	No connection.
42	NC	—	—	No connection.
43	NC	—	—	No connection.

No.	Pin Name	I/O	Type	Description
44	GH3	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
45	SH3	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
46	GL3	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
47	PGND2	I	Analog	Low-side MOSFET gate drive 3-4 sense and power return. Connect to system ground close to the device and half-bridge 3-4.
48	GL4	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
49	SH4	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
50	GH4	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
51	NC	—	—	No connection.
52	NC	—	—	No connection.
53	NC	—	—	No connection.
54	DGND	I/O	Ground	Device ground. Connect to system ground.
55	DVDD	I	Power	Device logic and digital output power supply input. External voltage reference and power supply for current sense amplifiers. Recommended to connect a 1.0-µF, 6.3-V ceramic capacitor between the DVDD and GND pins.
56	nSCS	I	Digital	Serial chip select. A logic low on this pin enables serial interface communication. Internal pullup resistor.

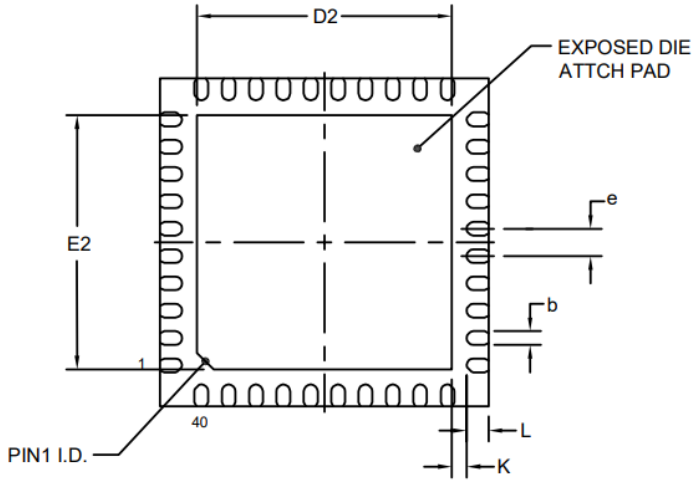
PACKAGE CASE OUTLINES



TOP VIEW



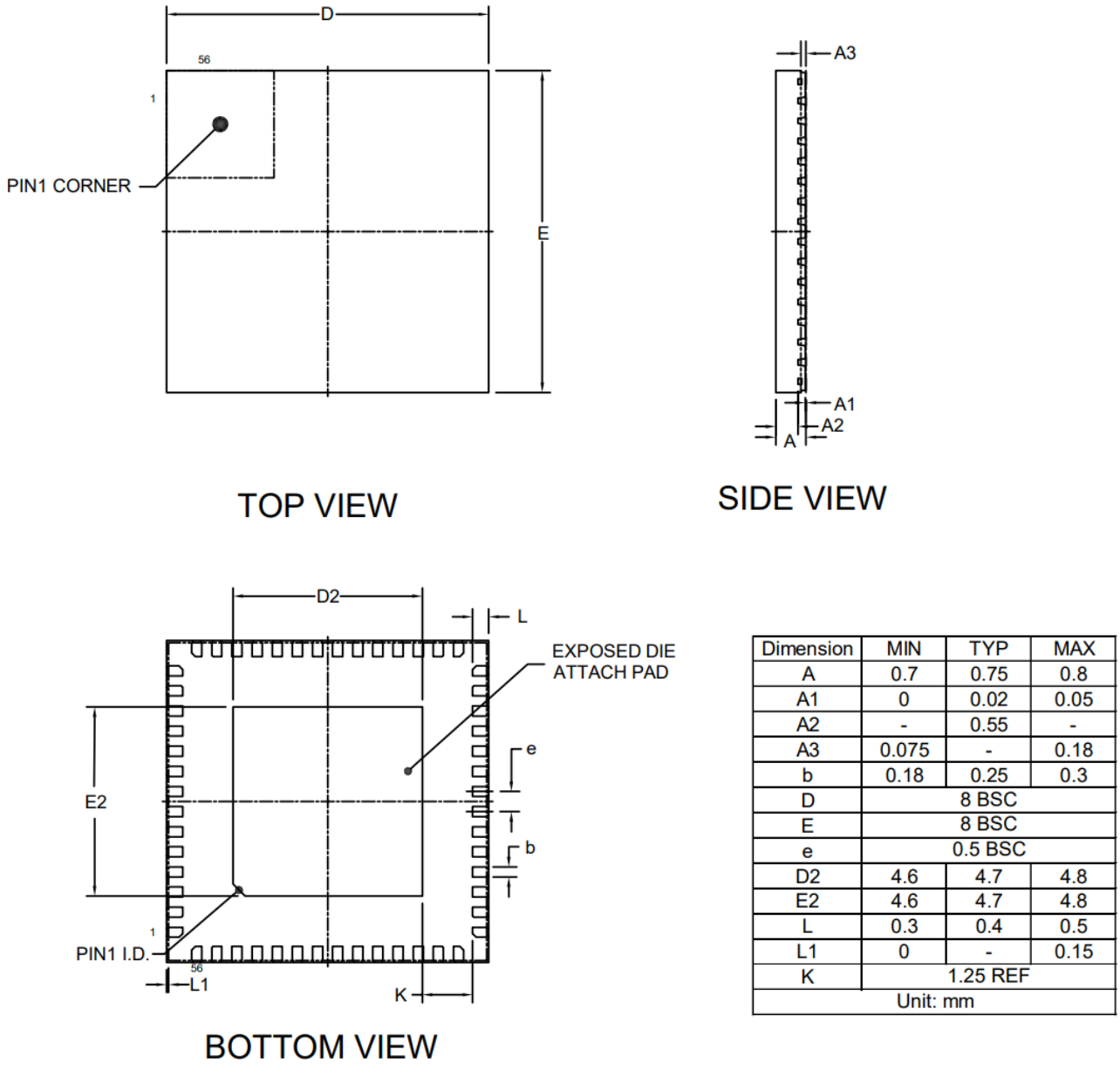
SIDE VIEW



BOTTOM VIEW

Dimension	MIN	TYP	MAX
A	0.8	0.85	1
A1	0	0.02	0.05
A2	-	0.65	-
b	0.18	0.25	0.3
D	6 BSC		
E	6 BSC		
e	0.5 BSC		
D2	4.6	4.65	4.7
E2	4.6	4.65	4.7
L	0.35	0.4	0.55
K	0.275REF		
Unit：mm			

Figure 3.QFN40 Package Outline Dimensions



Dimension	MIN	TYP	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.075	-	0.18
b	0.18	0.25	0.3
D	8 BSC		
E	8 BSC		
e	0.5 BSC		
D2	4.6	4.7	4.8
E2	4.6	4.7	4.8
L	0.3	0.4	0.5
L1	0	-	0.15
K	1.25 REF		
Unit: mm			

Figure 4.QFN56 Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Brief datasheet, Aug 2024	
Whole document	Brief datasheet Release