Dual Channel 10A, 5.0kV$_{RMS}$ Isolated Gate Driver

GENERAL DESCRIPTION

The SiLM8260A-AQ is an isolated dual channel gate driver with 10A source and 10A sink peak output current. The SiLM8260A-AQ are configured as high-side/low-side drivers with over-lap protection and programmable dead time feature. Pulling high the DIS pin shuts down both outputs simultaneously, and allows for normal operation when the DIS pin is open or pulled low. As a fail-safe measure, primary-side logic failures force both outputs low. The internal clamp feature to prevent false turn on caused by miller current.

The VDDA and VDDB supply voltage are up to 30 V. A wide input VDDI range from 3.5 V to 18 V makes the driver suitable for interfacing with both analog and digital controllers. All the supply voltage pins have under voltage lock-out (UVLO) protection.

The SiLM8260A-AQ has 5.0kV$_{RMS}$ isolation in SOP18W package per UL1577.

High CMTI, low propagation delay, small pulse width distortion and higher operation temperature makes the SiLM8260A-AQ ideal for use in all types of motor drives, solar inverters, industrial power supplies, and appliances.

FEATURE

- AEC-Q100 qualified for automotive application
  - Temperature grade 1: –40°C to +125°C, T_A
- 10A peak source/sink current
- 80ns (Typ.) propagation delay
- 150kV/us (Min.) common mode transient immunity (CMTI)
- Input side supply range from 3.5V to 18V
- Driver side supply range from 4V to 30V
  - 12.5V, 8.5V, 5.5V and 3.5V UVLO Options
- 5V reverse polarity voltage handling capability on input stage
- 1850V functional isolation between two drivers
- Safety certifications:
  - 5kV$_{RMS}$ isolation for 1 minute per UL 1577 with SOP18W package
  - CQC certification per GB4943.1-2011
  - DIN VDE 0884-17: 2021-10

APPLICATION

- AC/DC or DC/DC power supplies in server, telecom and industry
- DC/AC solar inverters
- EV battery charging

APPLICATION CIRCUIT

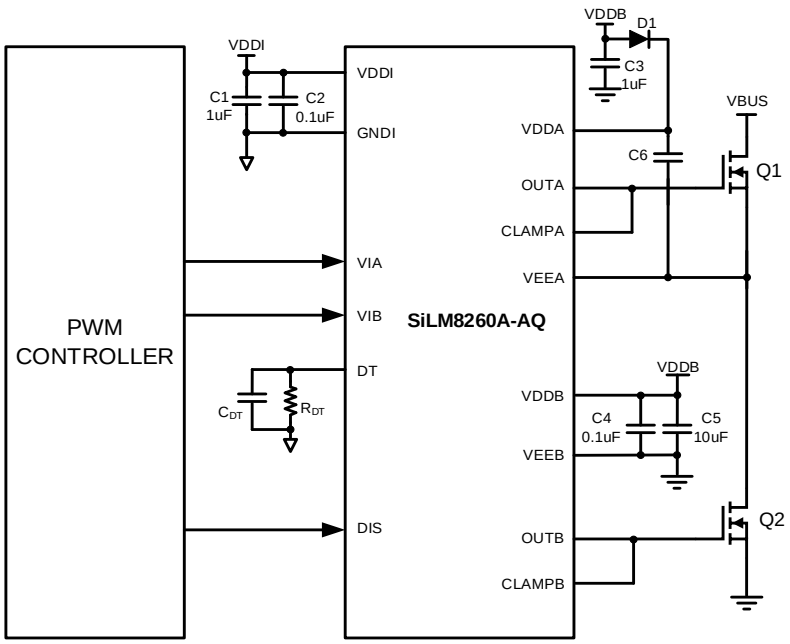

Figure 1. SiLM8260A-AQ Application Circuit

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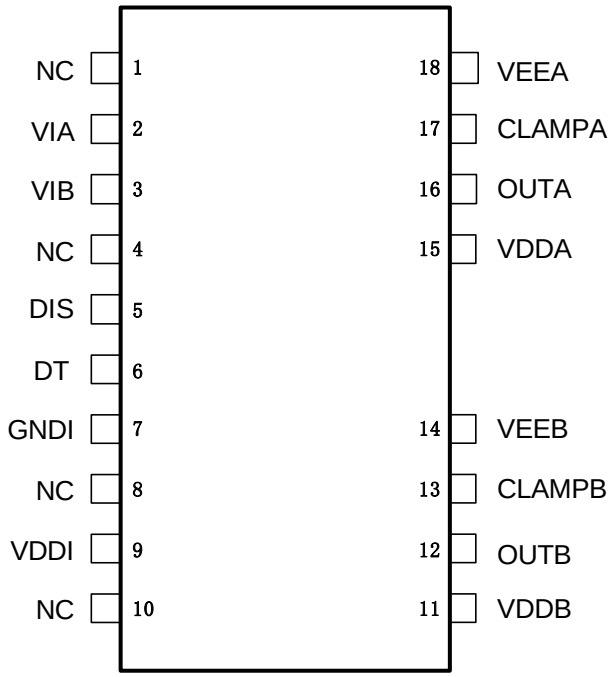
PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP18W	

PIN DESCRIPTION

No.	Pin Name	Description
1	NC	No connection
2	VIA	Input of driver A. The output of driver A is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
3	VIB	Input of driver B. The output of driver B is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
4	NC	No connection
5	DIS	Device disable input. When DIS pin is high, both driver is disabled and driver output is low. When DIS pin is low, it allows the device to perform in normal operation.
6	DT	Dead time programming input. Connect a resistor between DT and GNDI to program the dead time. A bypassing capacitor, 2.2nF or greater, is recommended to be put between DT and GNDI to achieve better noise immunity.
7	GNDI	Input power ground.
8	NC	No connection
9	VDDI	Input power supply. A local low ESR and ESL capacitor should be connected between VDDI and GNDI.
10	NC	No connection
11	VDDB	Power supply of driver B. A local low ESR and ESL capacitor should be connected between VDDB and VEEB.
12	OUTB	Output of driver B.
13	CLAMPB	Active Miller clamp input of driver B used to prevent false turn-on of the power switches
14	VEEB	Power ground of driver B.
15	VDDA	Power supply of driver A. A local low ESR and ESL capacitor should be connected between VDDA and VEEA.
16	OUTA	Output of driver A.
17	CLAMPA	Active Miller clamp input of driver A used to prevent false turn-on of the power switches
18	VEEA	Power ground of driver A.

FUNCTIONAL BLOCK DIAGRAM

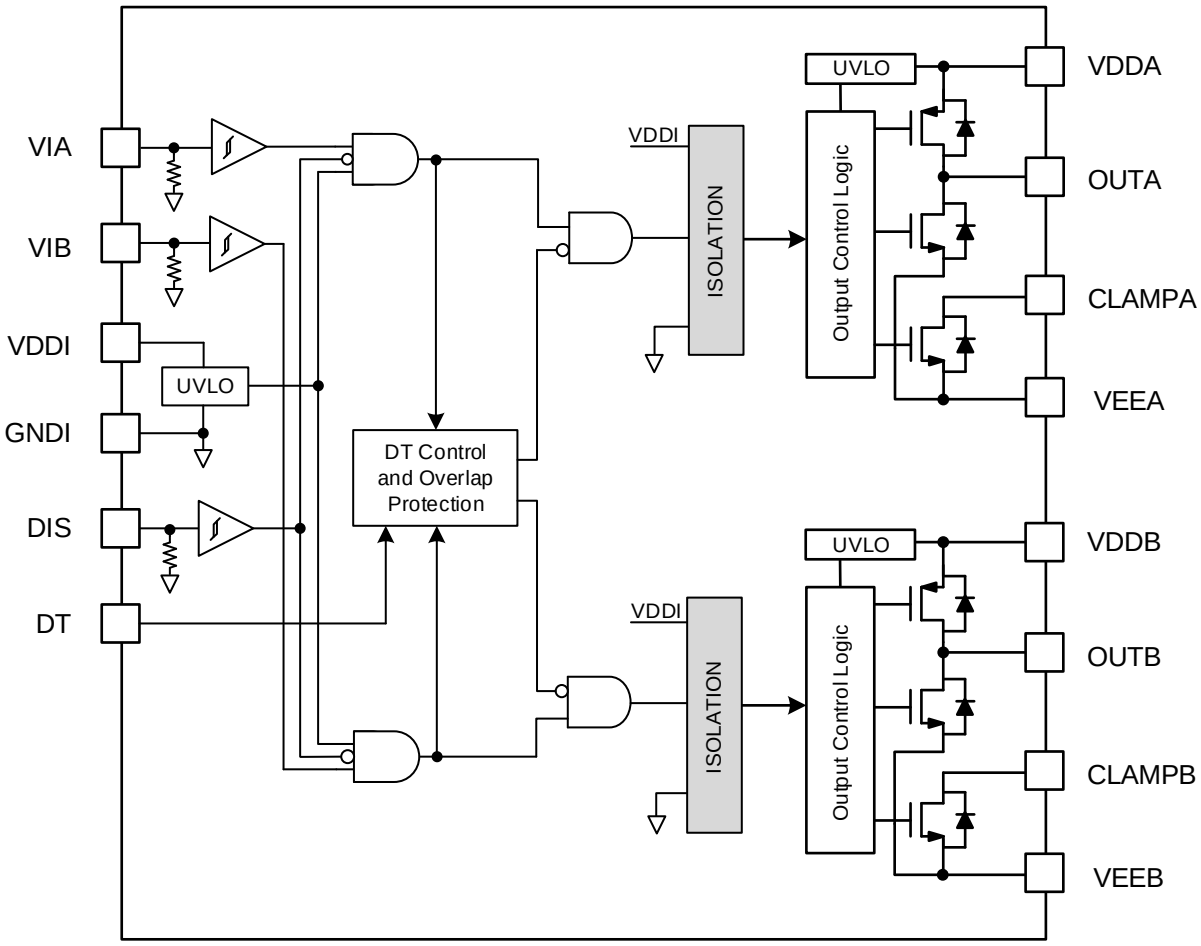


Figure 2. SiLM8260A-AQ Functional Block Diagram

ORDERING INFORMATION

Order Part No.	VCC2 UVLO	Package	QTY
SiLM8260ADCS-AQ	12.5V/11.5V	SOP18W	1500/Reel
SiLM8260ABCS-AQ	8.5V/7.5V	SOP18W	1500/Reel
SiLM8260AACS-AQ	5.5V/5V	SOP18W	1500/Reel
SiLM8260AGCS-AQ	3.5V/3V	SOP18W	1500/Reel

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Definition	Min	Max	Unit
V_{DDI}	Input Power Supply Voltage	-0.3	20	V
V_{IA}, V_{IB}, V_{DIS}	Input Signal Voltage	-7	20	V
V_{DDA}, V_{DDB}	Driver Power Supply	-0.3	35	V
V_{OUTA}, V_{OUTB}	Driver Output Voltage	-0.3	V_{DDA}+0.3, V_{DDB}+0.3	V
	Driver Output Voltage, Transient for 200ns[2]	-3	V_{DDA}+0.3, V_{DDB}+0.3	V
V_{CLAMPA}, V_{CLAMPB}	Internal Clamping Voltage	-0.3	V_{DDA}+0.3, V_{DDB}+0.3	V
	Internal Clamping Voltage, Transient for 200ns[2]	-3	V_{DDA}+0.3, V_{DDB}+0.3	V
V_{ch2ch}	Channel to Channel Internal Isolation Voltage		1850	V
T_J	Junction Temperature	-40	150	°C
T_S	Storage Temperature	-55	150	°C

RECOMMENDED OPERATION CONDITIONS[1]

Symbol	Definition	Min	Max	Unit
V_{DDI}	Input Power Supply Voltage	3.5	18	V
V_{IA}, V_{IB}, V_{DIS}	Input Signal Voltage	-5	18	V
V_{DDA}, V_{DDB}	Driver supply voltage (12.5V UVLO option)	13.6	30	V
	Driver supply voltage (8.5V UVLO option)	9.1	30	V
	Driver supply voltage (5.5V UVLO option)	6.0	30	V
	Driver supply voltage (3.5V UVLO option)	4.0	30	V
R_{DT}	Resistance range on DT	5	220	kΩ
C_{DT}	Capacitance on DT		10	nF
T_A	Ambient Temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM	±4000	V
	CDM	±2000	

Note 1: V_{DDI}, V_{IA}, V_{IB}, V_{DIS} are reference to GNDI; V_{DDA}, V_{OUTA}, V_{CLAMPA} are referenced to VEEA; V_{DDB}, V_{OUTB}, V_{CLAMPB} are referenced to VEEB;

Note 2: Values are verified by characterization on bench

THERMAL INFORMATION

Symbol	Definition	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	80	°C/W
$R_{\theta JC(TOP)}$	Junction to case (top) thermal resistance	35	°C/W

PACKAGE SPECIFICATIONS

Symbol	Definition	Min.	Typ.	Max.	Units
R_{IO}	Resistance (Input Side to Output Side)		10^{12}		Ω
C_{IO}	Capacitance (Input Side to Output Side)		1.8		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value	Units
CLR	External clearance	Shortest terminal to terminal distance through air	8.0	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	8.0	mm
DTI	Distance through the insulation	Minimum internal gap	>16	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	V
	Material Group		I	
	Overvoltage category	Rated mains voltages ≤150Vrms	IV	
		Rated mains voltages ≤300Vrms	IV	
		Rated mains voltages ≤600Vrms	III	
		Rated mains voltages ≤1000Vrms	II	
DIN VDE 0884-17(1)				
V_{IORM}	Maximum repetitive peak isolation voltage		1414	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (Sine wave)	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	60s	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC62368, 1.2/50us waveform, V_{TEST}=1.6 x V_{IOSM}	6250	V_{PK}
q_{pd}	Apparent charge	Method b2: $V_{pd(m)}$=1.875 x V_{IORM}, tm=1 s	≤5	pC
	Climatic Category		40/125/21	
	Pollution Degree		2	
UL1577(1)				
V_{ISO}	Withstand Isolation Voltage	V_{TEST}=V_{ISO}, t=60s (qualification), V_{TEST}=1.2 x V_{ISO}, t=1s (100% production)	5000	V_{RMS}

Note 1: Certification pending

SAFETY RELATED CERTIFICATIONS

VDE	UL	CQC
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2011
Reinforced Insulation	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude≤ 5000m, Tropical climate
Certification Pending	Certification Pending	Certification Pending

ELECTRICAL CHARACTERISTICS (DC)

V_{DDI} = 5 V, 0.1μF capacitor from VDDI to GNDI, V_{DDA} = V_{DDB} =15V, 1μF capacitor from VDDA and VDDB to VEEA and VEEB, T_A = –40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input Power Supply						
V_{DDI}	Input Supply Voltage		3.5		18	V
$V_{UVLO\_VDDI\_R}$	VDDI UVLO Rising		2.55	2.7	2.85	V
$V_{UVLO\_VDDI\_F}$	VDDI UVLO Falling		2.35	2.5	2.65	V
V_{UVLO_HYS}	VDDI UVLO Hysteresis			0.2		V
I_{VDDI}	Quiescent Current	V_{IA} = 0V, V_{IB} = 0V	1.4	2	2.6	mA
	Operation Current	f_{sw}= 50kHz, (50% Duty Cycle), both channels	2.17	3.1	4.03	mA
Logic Interface						
V_{IH}	High Level Input Threshold Voltage at VIA, VIB and DIS			2.5	3	V
V_{IL}	Low Level Input Threshold Voltage at VIA, VIB and DIS		1	1.4		V
V_{IHYS}	Hysteresis Voltage at VIA, VIB and DIS			1.1		V
R_{PD}	Pull down Resistance on VIA,VIB and DIS		126	180	235	kΩ
Driver Power Supply						
$V_{UVLO\_VDDA\_R}$, $V_{UVLO\_VDDB\_R}$	VDDA, VDDB UVLO Rising	3.5V UVLO Version	3.2	3.5	3.8	V
		5.5V UVLO Version	5.1	5.5	5.9	V
		8.5V UVLO Version	8	8.5	9	V
		12.5V UVLO Version	11.5	12.5	13.5	V
$V_{UVLO\_VDDA\_F}$, $V_{UVLO\_VDDB\_F}$	VDDA, VDDB UVLO Falling	3.5V UVLO Version	2.7	3	3.3	V
		5.5V UVLO Version	4.6	5	5.4	V
		8.5V UVLO Version	7	7.5	8	V
		12.5V UVLO Version	10.5	11.5	12.5	V
$V_{UVLO\_VDDA\_HYS}$, $V_{UVLO\_VDDB\_HYS}$	VDDA, VDDB UVLO Hysteresis	3.5V UVLO Version		0.5		V
		5.5V UVLO Version		0.5		V
		8.5V UVLO Version		1		V
		12.5V UVLO Version		1		V
I_{VDDA_Q}, I_{VDDB_Q}	VDDA/B Quiescent Current, per Channel	V_{IA} = 0V, V_{IB} = 0V		1.4	2.1	mA
I_{VDDA_OP}, I_{VDDB_OP}	VDDA/B Operation Current, per Channel	C_{LOAD}=1nF, f_{sw}= 50kHz, (50% Duty Cycle)		2.7	3.5	mA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
OUTPUT						
I_{OH}	Peak Source Current			10		A
I_{OL}	Peak Sink Current			10		A
V_{OH}	High Level Output Voltage	I_O=-20mA		8	15	mV
V_{OL}	Low Level Output Voltage	I_O=20mA		8	15	mV
V_{OUTSD}	Active pulldown voltage on OUTA(B)	I_{OUT}=0.1A, VDDA(B) Open		1.8	2.5	V
Active Miller Clamp						
I_{CLAMP}	Clamp low level current			10		A
V_{CLAMP}	Clamp low level voltage	I_{CLAMP}=20mA		7	13	mV
$V_{CLAMP-TH}$	Clamp threshold voltage		1.8	2	2.2	V
Dead Time						
t_{DT}	Dead time	R_{DT}=20kΩ	160	200	250	ns

SWITCHING CHARACTERISTICS (AC)

V_{DDI} = 5 V, 0.1μF capacitor from VDDI to GNDI, V_{DDA} = V_{DDB} =15V, 1μF capacitor from VDDA and VDDB to VEEA and VEEB, T_A = –40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation delay, Low to High	C_{LOAD}=1nF, f_{sw}=20kHz, (50% Duty Cycle)		80	130	ns
t_{PHL}	Propagation delay, High to Low			80	130	ns
t_{PWD}	Pulse Width Distortion				40	ns
t_{DM}	Propagation Delay Matching between OUTA and OUTB				40	ns
t_r	Turn on rise time	C_{LOAD}=1nF			15	ns
t_f	Turn off fall time	C_{LOAD}=1nF			15	ns
$t_{UVLO\_REC\_VDDI}$	VDDI UVLO Recovery Delay			15		us
$t_{UVLO\_REC\_VDDA(B)}$	VDDA, VDDB UVLO Recovery Delay			25	40	us
$CMTI_H$	Output High Level Common Mode Transient Immunity	V_{CM}=1000V, $V_{DDA(B)}$=15V, T_A=25°C	150	200		kV/us
$CMTI_L$	Output Low Level Common Mode Transient Immunity	V_{CM}=1000V, $V_{DDA(B)}$=15V, T_A=25°C	150	200		kV/us

PARAMETER MEASUREMENT INFORMATION

Propagation Delay and Pulse Width Distortion

Figure 3 shows the timing diagram of the propagation delay t_{PLH} and t_{PHL}, pulse distortion t_{PWD} and delay matching t_{DM} from the input V_{IA} and V_{IB}. Short the DT pin to VDDI to disable the dead time function.

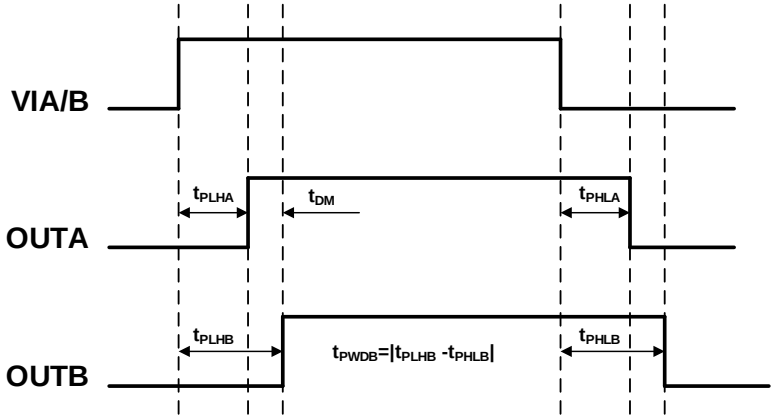


Figure 3. Propagation Delay and Pulse Width Distortion

Rise and Fall Time Testing

Figure 4 shows the criteria for measuring rise time (t_r) and fall time (t_f).

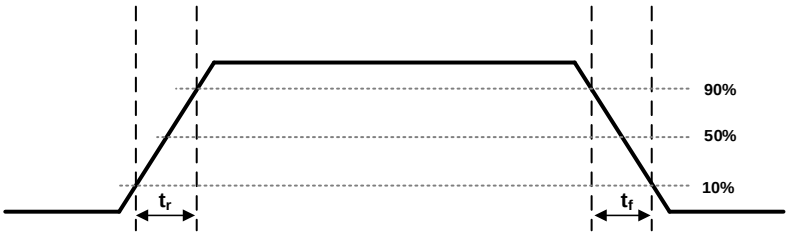


Figure 4. Turn On Rise Time and Turn Off Fall Time

CMTI Testing

Figure 5 is the simplified diagram of the CMTI testing. Common mode voltage is set to 1000V.

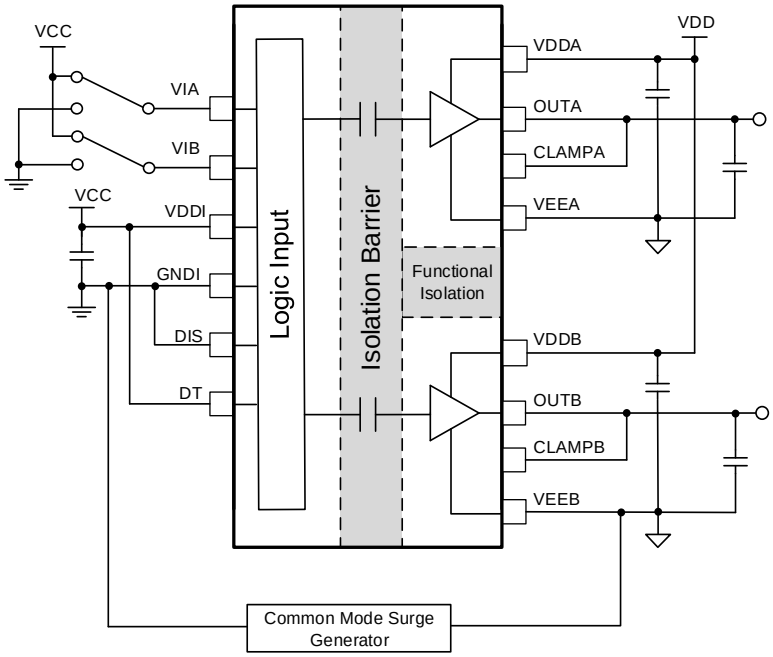


Figure 5. CMTI Test Circuit

FEATURE DESCRIPTION

SiLM8260A-AQ is a flexible dual channel isolated gate driver that can drive IGBTs and MOSFETs. It has 10A peak output current capability with maxim output driver supply voltage of 30V. SiLM8260A-AQ has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor programmable dead time control, an DIS pin, and under voltage lock out (UVLO) for both input and output voltages.

Under Voltage Lockout

The SiLM8260A-AQ has under voltage lock out (UVLO) protection feature on each driver power supply voltage between the VDDA (VDDB) and VEEA (VEEB) pins. When the VDDx voltage is lower than $V_{UVLO\_VDDX\_R}$, during device start up or lower than $V_{UVLO\_VDDX\_F}$, after start up, the VDDA (VDDB) UVLO feature holds the driver output low, regardless of the status of the input pins. A hysteresis on the UVLO feature prevents glitch when there is noise from the power supply.

The SiLM8260A-AQ also monitors the input power supply and there is an internal under voltage lock out protection feature on the VDDI. The driver outputs (OUTA and OUTB) are hold low when the voltage on the VDDI is lower than $V_{UVLO\_VDDI\_R}$ during start up or lower than $V_{UVLO\_VDDI\_F}$ after start up. There is a hysteresis on the VDDI UVLO feature to prevent glitch due the noise on the VDDI power supply.

Disable Input Function

When the DIS is pulled high, the OUTA and OUTB are pulled low regardless of the states of VIA and VIB. When the DIS pin is pulled low, the OUTA and OUTB are allowed for normal operation and controlled by the VIA and VIB.

The DIS input has no effect if VDDI is below its UVLO threshold and OUTA, OUTB remains low. There is an internal pull down resistor on the DIS pin.

Control Input and Output Logic

The VIA and VIB input control the corresponding output channel, OUTA and OUTB. A logic high signal on VIA (VIB) causes the output of OUTA (OUTB) to go high. And a logic low on VIA (VIB) causes the output of OUTA (OUTB) to go low.

The Table 1 shows the relationship between VIA, VIB, DIS, UVLO and Output of OUTA and OUTB.

Table 1. Relationship between Input and Output with VIA, VIB input

VIA	VIB	DIS	VDDI UVLO	VDDA UVLO	VDDB UVLO	OUTA	OUTB	Note
H	L	L	No	No	No	H	L	
L	H	L	No	No	No	L	H	
L	L	L	No	No	No	L	L	
H	H	L	No	No	No	L	L	
X	X	H	No	No	No	L	L	Device disabled
X	X	X	Yes	No	No	L	L	VDDI UVLO active
H	X	L	No	No	Yes	H	L	VDDB UVLO active
L	X	L	No	No	Yes	L	L	
X	H	L	No	Yes	No	L	H	VDDA UVLO active
X	L	L	No	Yes	No	L	L	

Dead-time Program

There is a dead-time between OUTA and OUTB. The dead-time delay (t_{DT}) is programmed by a resistor (R_{DT}) connected from the DT input to ground and it can be calculated with below equation.

$$t_{DT}[\text{ns}] \approx 10\times R_{DT}[\text{k}\Omega]$$

Here, t_{DT} is the dead-time delay, R_{DT} is the resistance value between DT and ground.

The DT pin can be connected to VDDI or left floating to provide a nominal dead time at approximately 400 ps.

A bypassing capacitor, 2.2nF or greater, is recommended to be put between DT and GNDI to achieve better noise immunity.

The Figure 6 shows the input and output logic with dead-time in different condition.

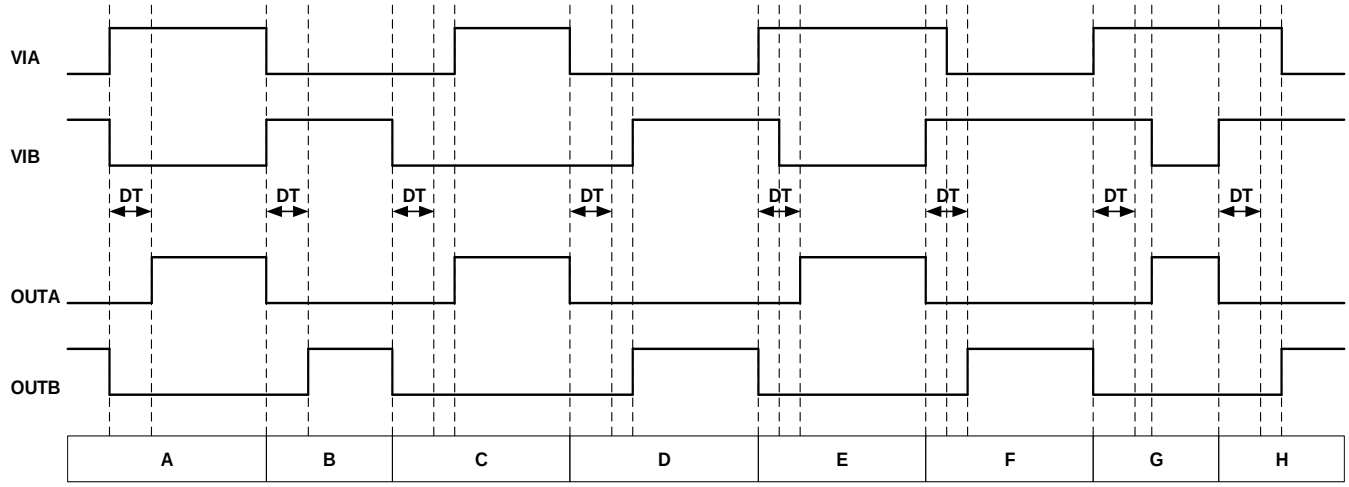


Figure 6. Input and output logic with dead-time

Condition A: VIA goes high and VIB goes low. OUTB goes low immediately and OUTA goes high after the programmed dead-time.

Condition B: VIA goes low and VIB goes high. OUTA goes low immediately and OUTB goes high after the programmed dead-time.

Condition C: VIB goes low and VIA still low. OUTB goes low immediately. Since the VIA input dead-time is longer than the programmed dead-time, the OUTA goes high immediately when the VIA input goes high.

Condition D: VIA goes low and VIB still low. OUTA goes low immediately. Since the VIB input dead-time is longer than the programmed dead-time, the OUTB goes high immediately when the VIB input goes high.

Condition E: VIA goes high while VIB and OUTB are still high, the overlap time is shorter than the programmed dead- time. To avoid overshoot, OUTB goes low immediately when the VIA goes high. The OUTA goes high after the programmed dead-time.

Condition F: VIB goes high while VIA and OUTA are still high, the overlap time is shorter than the programmed dead-time. To avoid overshoot, OUTA goes low immediately when the VIB goes high. The OUTB goes high after the programmed dead-time.

Condition G: VIA goes high while VIB and OUTB are still high, the overlap time is longer than the programmed dead- time. To avoid overshoot, OUTB goes low immediately when the VIA goes high. Since the overlap time is longer than the programmed dead-time, the OUTA goes high immediately when the VIB goes low.

Condition H: VIB goes high while VIA and OUTA are still high, the overlap time is longer than the programmed dead-time. To avoid overshoot, OUTA goes low immediately when the VIB goes high. Since the overlap time is longer than the programmed dead-time, the OUTB goes high when the VIA goes low.

Internal Active Miller Clamp

A Miller clamp circuit integrates in the SiLM8260A-AQ which allows the control of the Miller current during a high dV/dt situation and can eliminate the use of a negative supply voltage in most of the applications. During turn off, the gate voltage is monitored through the CLAMPA(B) and the clamp circuit is activated when the voltage on the CLAMPA(B) pin goes below the clamp voltage threshold (2V typical, relative to VEEA(B)). A clamp low sink current is generated when the clamp circuit is activated. The clamp circuit is disabled when the input on signal is triggered again.

Active Output Pulldown

The active output pulldown feature ensures that the OUTA(B) is clamped to approximately 1.8V higher than VEE2 to ensure safe IGBT off-state during VDDA(B) is open.

APPLICATION INFORMATION

The circuit in Figure 7 shows the typical application circuit for SiLM8260A-AQ to driver a typical half bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half bridge, full bridge, LLC etc. topologies and 3-phase motor drive applications.

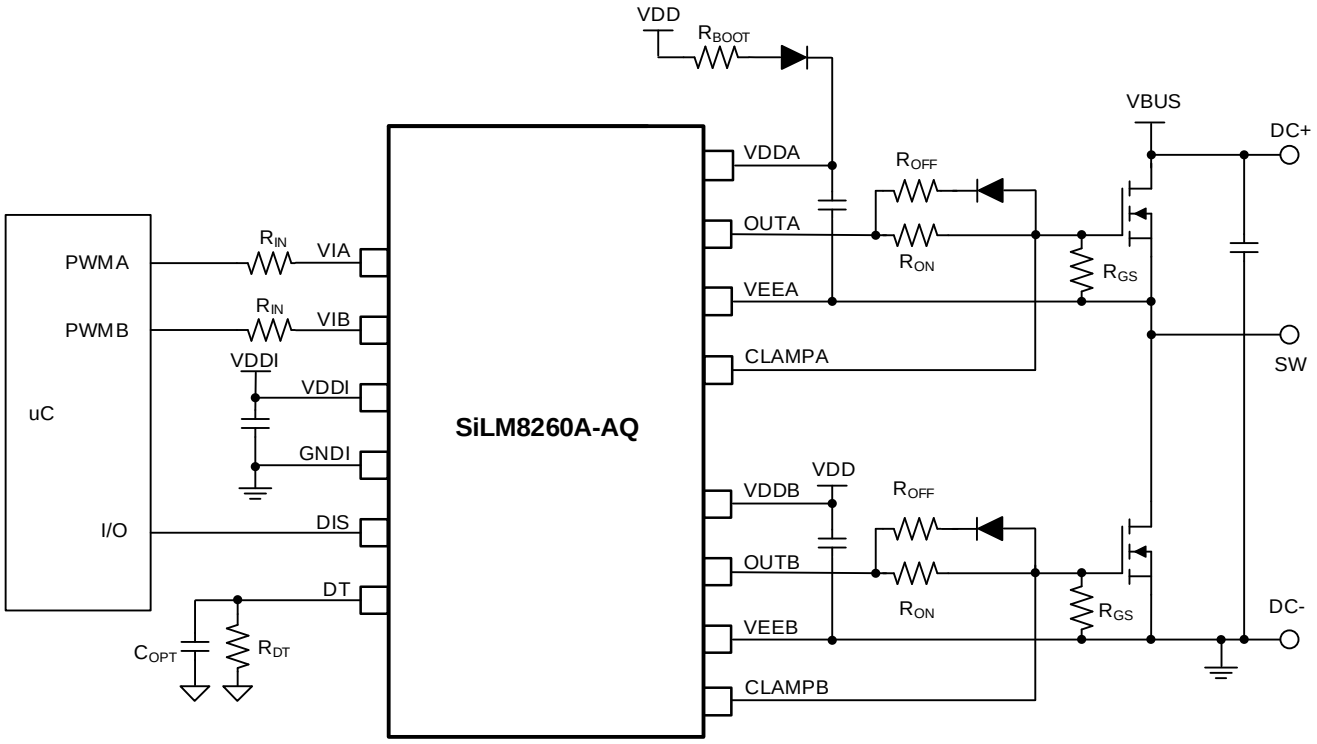
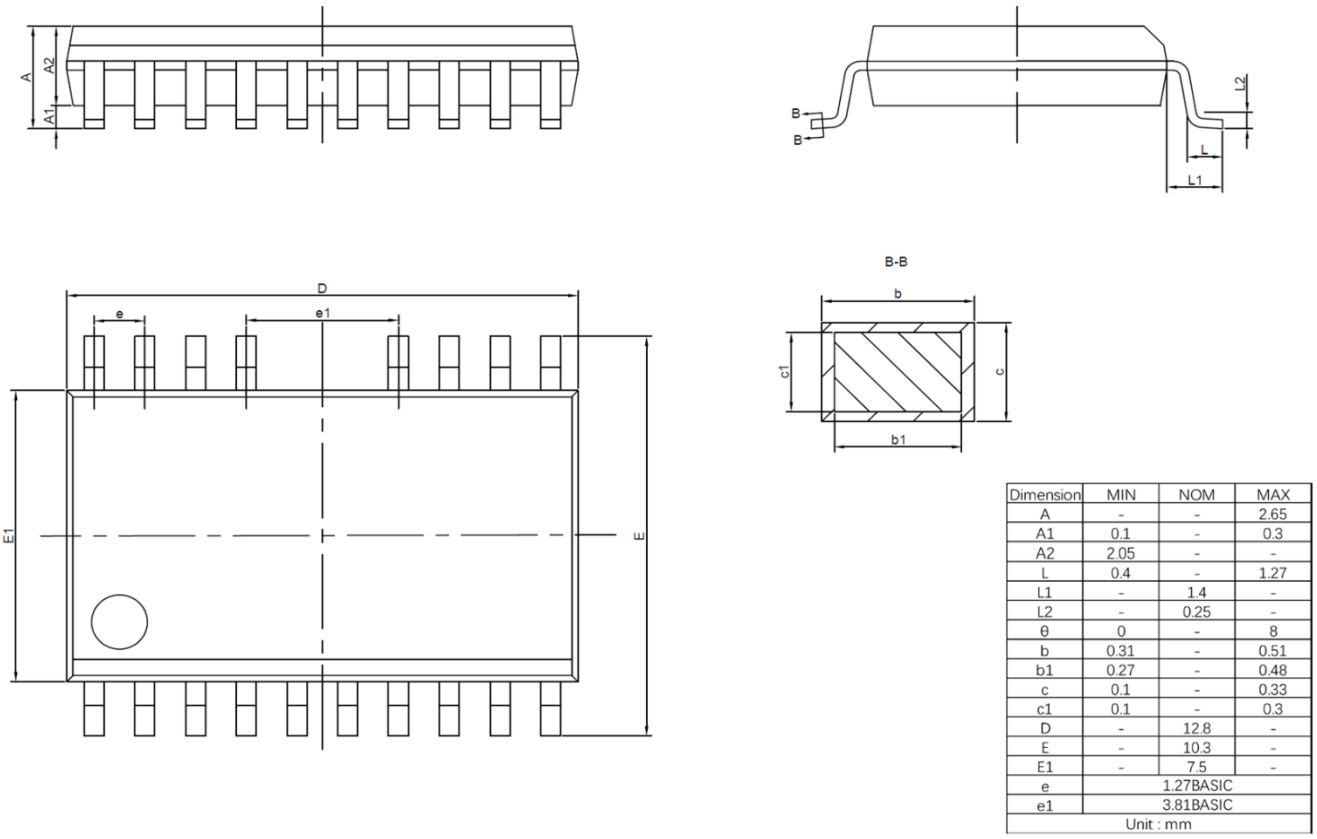


Figure 7. Typical Application Schematic

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	2.65
A1	0.1	-	0.3
A2	2.05	-	-
L	0.4	-	1.27
L1	-	1.4	-
L2	-	0.25	-
θ	0	-	8
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.1	-	0.33
c1	0.1	-	0.3
D	-	12.8	-
E	-	10.3	-
E1	-	7.5	-
e	1.27BASIC		
e1	3.81BASIC		
Unit : mm			

Figure 8. SOP18W Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: 2023-10-15	
Whole document	Initial datasheet release
Rev 1.1 datasheet: 2024-11-28	
Page 12	Update the parameters: t_{PLH}, t_{PHL}, t_{PW}, t_{DM} and t_{DT}.