Six Channel Digital Isolator with Integrated Interlock

GENERAL DESCRIPTION

The SiLM5768L and SiLM5768LN are high performance, six channel digital isolator with 5.0 kV_{RMS} isolation rating per UL1577. The devices provide high electromagnetic immunity and low emissions at low power consumption.

The SiLM5768L/SiLM5768LN has all channels in the same direction and it integrates the interlock functionality for adjacent channels. The interlock feature ensures that each channel, in a channel pairing, will not be enabled at the same time. If both channels in the pairing share the same input logic, the output logic will always be low.

The SiLM5768L and SiLM5768LN are available in SOP16W package and support wide operation temperature from –40°C to +125°C.

APPLICATION

- Motor drivers
- Appliances
- Grid
- Building automation

FEATURES

- Integrated interlock function
  - Support opposite polarity of adjacent channels
  - Three sets of paired interlock channels
- Channel output non-inverting in SiLM5768L and inverting in SiLM5768LN
- Data rate up to 100Mbps
- Propagation delay 13ns (Typ)
- CMTI 150kV/us (Typ)
- Low power consumption: 1.4mA/Channel (Typ) at 1Mbps
- Wide supply voltage: 2.25V to 5.5V
- 2.25V to 5.5V level translation
- Robust electromagnetic compatibility (EMC)
  - System Level ESD, EFT, and surge immunity
  - Low emissions
- Operation temperature: –40°C to +125°C
- SOP16W package
- Safety certifications:
  - 5.0kV_{RMS} isolation for 1 minute per UL 1577
  - CQC certification per GB4943.1-2022
  - DIN VDE 0884-17: 2021-10

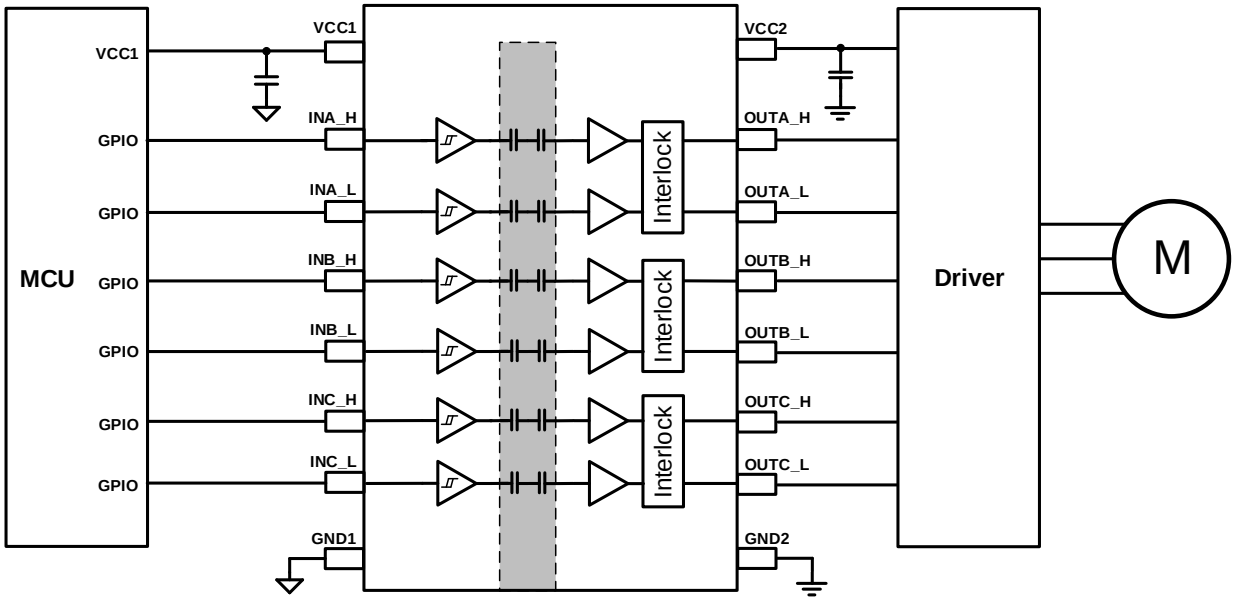

Figure 1. SiLM5768L Typical Application Circuit

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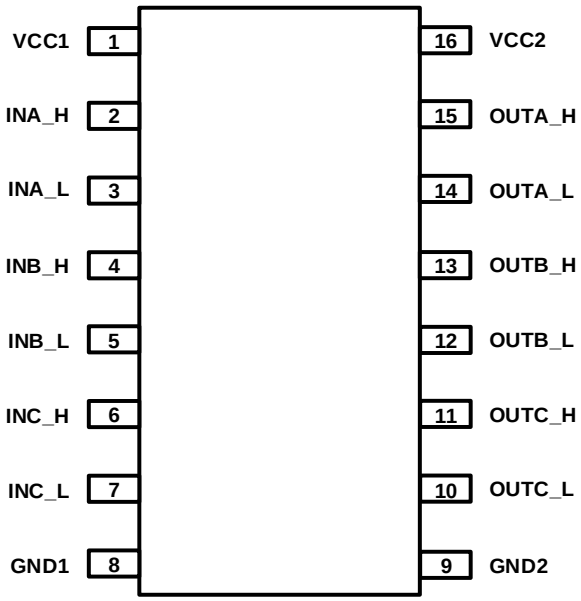
PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP16W	

PIN DESCRIPTION

Pin No.	Pin Name	Description
1	VCC1	Power supply for side1.
2	INA_H	Channel A_H input. Interlock paired with channel A_L.
3	INA_L	Channel A_L input. Interlock paired with channel A_H.
4	INB_H	Channel B_H input. Interlock paired with channel B_L.
5	INB_L	Channel B_L input. Interlock paired with channel B_H.
6	INC_H	Channel C_H input. Interlock paired with channel C_L.
7	INC_L	Channel C_L input. Interlock paired with channel C_H.
8	GND1	Power ground for side1.
9	GND2	Power ground for side2.
10	OUTC_L	Channel C_L output. Interlock paired with channel C_H.
11	OUTC_H	Channel C_H output. Interlock paired with channel C_L.
12	OUTB_L	Channel B_L output. Interlock paired with channel B_H.
13	OUTB_H	Channel B_H output. Interlock paired with channel B_L.
14	OUTA_L	Channel A_L output. Interlock paired with channel A_H.
15	OUTA_H	Channel A_H output. Interlock paired with channel A_L.
16	VCC2	Power supply for side2.

FUNCTIONAL BLOCK DIAGRAM

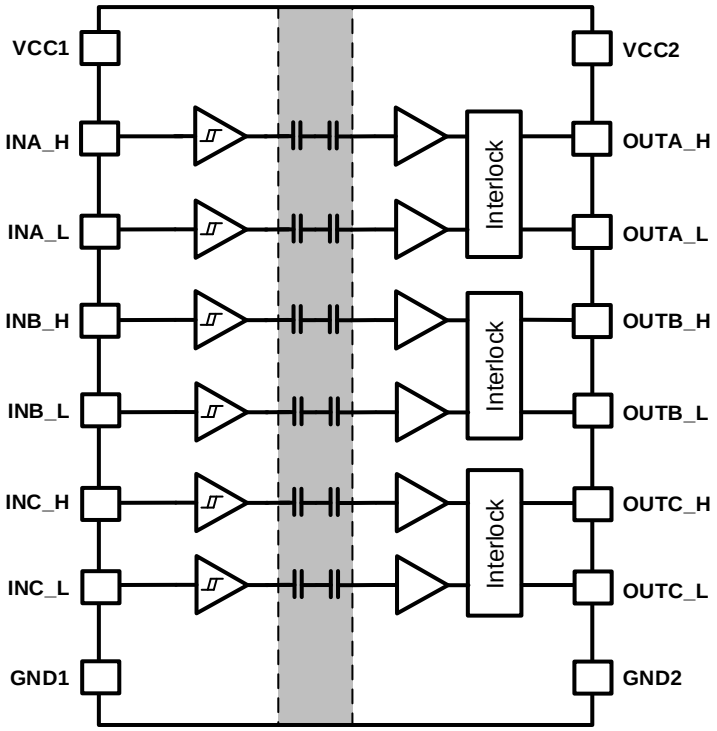


Figure 2. SiLM5768L/SiLM5768LN Functional Block

ORDERING INFORMATION

Order Part No.	Package	QTY
SiLM5768LCG-DG	SOP16W, Pb-Free	1500/Reel
SiLM5768LNCG-DG	SOP16W, Pb-Free	1500/Reel

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V_{CC1}, V_{CC2}	Supply voltage, VCC1 and VCC2	-0.3	6	V
V_I	Voltage at INx, referenced to GND1	-0.3	V_{CC1}+0.3	V
V_{OUT}	Voltage at OUTx, reference to GND2	-0.3	V_{CC2}+0.3	V
I_O	Output Current	-15	15	mA
T_J	Junction temperature	-55	150	°C
T_S	Storage temperature	-65	150	°C

Note:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the Recommended Operation Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All voltage parameters are referenced to local ground terminal, GND1 or GND2.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V_{CC1}, V_{CC2}	Supply voltage	2.25	5.5	V
I_{OH}	High level output current @ V_{CC2}=5V	-4		mA
	High level output current @ V_{CC2}=3.3V	-2		mA
	High level output current @ V_{CC2}=2.5V	-1		mA
I_{OL}	Low level output current @ V_{CC2}=5V		4	mA
	Low level output current @ V_{CC2}=3.3V		2	mA
	Low level output current @ V_{CC2}=2.5V		1	mA
V_{IH}	High Level Input Voltage	0.7× V_{CC1}	V_{CC1}	V
V_{IL}	Low Level Input Voltage	0	0.3× V_{CC1}	V
DR	Data Rate	0	100	Mbps
T_A	Ambient temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM	±8000	V
	CDM	±2000	V

THERMAL INFORMATION

Symbol	Definition	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	83.5	°C/W
$R_{\theta JC}$	Junction to case (top) thermal resistance	40	°C/W

PACKAGE SPECIFICATIONS

Symbol	Definition	Min.	Typ.	Max.	Units
R_{IO}	Resistance (Input Side to Output Side)		10^{12}		Ω
C_{IO}	Capacitance (Input Side to Output Side)		1		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value	Units
CLR	External clearance	Shortest terminal to terminal distance through air	>8.0	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	>8.0	mm
DTI	Distance through the insulation	Minimum internal gap	>16	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	V
	Material Group		I	
	Overvoltage category	Rated mains voltage ≤150V_{RMS}	I-IV	
		Rated mains voltage ≤300 V_{RMS}	I-IV	
		Rated mains voltage ≤600 V_{RMS}	I-III	
		Rated mains voltage ≤1000 V_{RMS}	I-II	
DIN V VDE 0884-11(1)				
V_{IORM}	Maximum repetitive peak isolation voltage		1414	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (Sine wave)	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	60s	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC62368, 1.2/50us waveform, V_{TEST}=1.6 x V_{IOSM}	6250	V_{PK}
q_{pd}	Apparent charge		≤5	pC
	Climatic Category		40/125/21	
	Pollution Degree		2	
UL1577(1)				
V_{ISO}	Withstand Isolation Voltage	V_{TEST}=V_{ISO}, t=60s (qualification), V_{TEST}=1.2 x V_{ISO}, t=1s (100% production)	5000	V_{RMS}

Note1: Certification pending

SAFETY RELATED CERTIFICATIONS

VDE	UL	CQC
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022
Reinforced Insulation	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude≤ 5000m, Tropical climate
Pending	Pending	File number: CQC23001379622

SAFETY LIMITING VALUES

Symbol	Parameter	Condition	Value	Unit
I_S	Safety input, output, or supply current	$R_{\theta JA}$=83.5°C/W, V_{CC1}=V_{CC2}=5V, T_J=150°C, T_A=25°C	299	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$=83.5°C/W, V_{CC1}=V_{CC2}=5V, T_J=150°C, T_A=25°C	1496	mW
T_S	Maximum safety temperature		150	°C

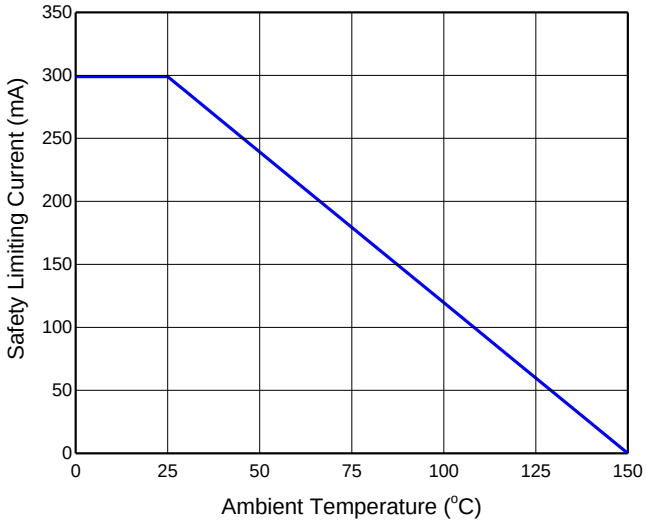


Figure 3. Thermal Derating Curve for Limiting Current per VDE

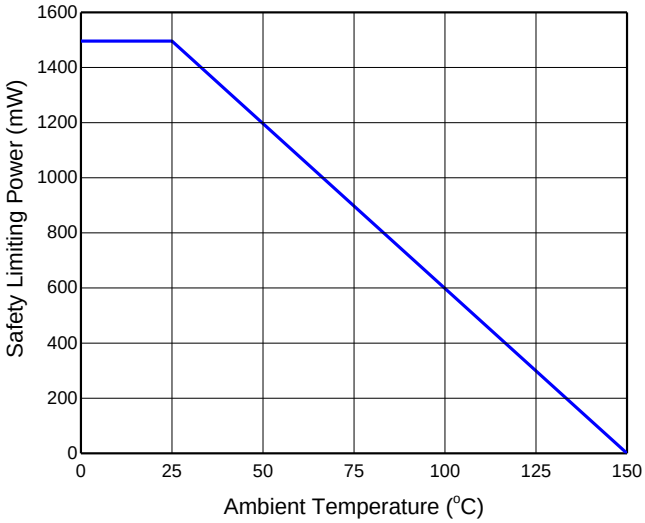


Figure 4. Thermal Derating Curve for Limiting Power per VDE

ELECTRICAL CHARACTERISTICS (DC) WITH 5V SUPPLY

V_{CC1} = V_{CC2}=5V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
Power Supply UVLO						
$UVLO_R$	Under Voltage Lockout V_{CCx} rising			2.05	2.25	V
$UVLO_F$	Under Voltage Lockout V_{CCx} falling		1.7	1.9		V
$UVLO_{HYS}$	Under Voltage Lockout Hysteresis			0.15		V
Power Supply Current						
I_{CC1_Q}	Current on VCC1 with complementary input	V_{IH} = V_{CC1} ,V_{IL} = 0V or V_{IH} = 0V ,V_{IL} = V_{CC1}		4.4	6.0	mA
I_{CC2_Q}	Current on VCC2 with complementary input			3.3	4.6	mA
$I_{CC1\_OP\_1M}$	Current on VCC1 at 1Mbps	1 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.4	7.0	mA
$I_{CC1\_OP\_10M}$	Current on VCC1 at 10Mbps	10 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.4	7.0	mA
$I_{CC1\_OP\_50M}$	Current on VCC1 at 50Mbps	50 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.8	7.7	mA
$I_{CC1\_OP\_100M}$	Current on VCC1 at 100Mbps	100 Mbps, C_L = 15pF, all channel switching with square wave clock input		5.1	8.2	mA
$I_{CC2\_OP\_1M}$	Current on VCC2 at 1Mbps	1 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.1	6.6	mA
$I_{CC2\_OP\_10M}$	Current on VCC2 at 10Mbps	10 Mbps, C_L = 15pF, all channel switching with square wave clock input		10.5	16.8	mA
$I_{CC2\_OP\_50M}$	Current on VCC2 at 50Mbps	50 Mbps, C_L = 15pF, all channel switching with square wave clock input		26.9	37.5	mA
$I_{CC2\_OP\_100M}$	Current on VCC2 at 100Mbps	100 Mbps, C_L = 15pF, all channel switching with square wave clock input		44.0	61.5	mA
Input Logic Interface						
V_{IH}	Rising input threshold voltage			0.6× V_{CC1}	0.7× V_{CC1}	V

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
V_{IL}	Falling input threshold voltage		0.3× V_{CC1}	0.4× V_{CC1}		V
V_{IHYS}	Input threshold voltage hysteresis			0.2× V_{CC1}		V
I_{IH}	High level input current	V_{INx} = V_{CC1}			10	uA
I_{IL}	Low level input current	V_{INx} = 0V	-10			uA
Output Logic Interface						
V_{OH}	High level output voltage	I_{OH} = -4mA	V_{CC2} -0.4	4.8		V
V_{OL}	Low level output voltage	I_{OL} = 4mA		0.12	0.3	V
CMTI						
$CMTI_H$	Output High Level Common Mode Transient Immunity	V_I = V_{CC1}, V_{CM}=1200V, C_L=15pF		150		kV/us
$CMTI_L$	Output Low Level Common Mode Transient Immunity	V_I = 0V, V_{CM}=1200V, C_L=15pF		150		kV/us

SWITCHING CHARACTERISTICS (AC) WITH 5V SUPPLY

V_{CC1} = V_{CC2}=5V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay, Low to High	C_L=15pF		13	25	ns
t_{PHL}	Propagation delay, High to Low	C_L=15pF		13	25	ns
t_r	Turn on rise time	C_L=15pF		2		ns
t_f	Turn off fall time	C_L=15pF		2		ns
t_{PWD}	Pulse Width Distortion	C_L=15pF			10	ns
t_{SKO}	Channel to Channel Output Skew Time	C_L=15pF, same direction in single device			8	ns
t_{SKP}	Part to Part Skew Time	C_L=15pF, same direction			8	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC1} goes below 1.7V		0.15		us

ELECTRICAL CHARACTERISTICS (DC) WITH 3.3V SUPPLY

V_{CC1} = V_{CC2}=3.3V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
Power Supply UVLO						
$UVLO_R$	Under Voltage Lockout V_{CCx} rising			2.05	2.25	V
$UVLO_F$	Under Voltage Lockout V_{CCx} falling		1.7	1.9		V
$UVLO_{HYS}$	Under Voltage Lockout Hysteresis			0.15		V
Power Supply Current						
I_{CC1_Q}	Current on VCC1 with complementary input	V_{IH} = V_{CC1} , V_{IL} = 0V or V_{IH} = 0V , V_{IL} = V_{CC1}		4.3	5.9	mA
I_{CC2_Q}	Current on VCC2 with complementary input			3.2	4.6	mA
$I_{CC1\_OP\_1M}$	Current on VCC1 at 1Mbps	1 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.3	6.5	mA
$I_{CC1\_OP\_10M}$	Current on VCC1 at 10Mbps	10 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.4	7.0	mA
$I_{CC1\_OP\_50M}$	Current on VCC1 at 50Mbps	50 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.6	7.5	mA
$I_{CC1\_OP\_100M}$	Current on VCC1 at 100Mbps	100 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.9	7.8	mA
$I_{CC2\_OP\_1M}$	Current on VCC2 at 1Mbps	1 Mbps, C_L = 15pF, all channel switching with square wave clock input		3.5	5.6	mA
$I_{CC2\_OP\_10M}$	Current on VCC2 at 10Mbps	10 Mbps, C_L = 15pF, all channel switching with square wave clock input		6.1	9.7	mA
$I_{CC2\_OP\_50M}$	Current on VCC2 at 50Mbps	50 Mbps, C_L = 15pF, all channel switching with square wave clock input		15.9	22.3	mA
$I_{CC2\_OP\_100M}$	Current on VCC2 at 100Mbps	100 Mbps, C_L = 15pF, all channel switching with square wave clock input		26.5	37.5	mA
Input Logic Interface						
V_{IH}	Rising input threshold voltage			0.6× V_{CC1}	0.7× V_{CC1}	V

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
V_{IL}	Falling input threshold voltage		0.3× V_{CC1}	0.4× V_{CC1}		V
V_{IHYS}	Input threshold voltage hysteresis			0.2× V_{CC1}		V
I_{IH}	High level input current	V_{INx} = V_{CC1}			10	uA
I_{IL}	Low level input current	V_{INx} = 0V	-10			uA
Output Logic Interface						
V_{OH}	High level output voltage	I_{OH} = -2mA	V_{CC2} - 0.3	3.2		V
V_{OL}	Low level output voltage	I_{OL} = 2mA		0.07	0.2	V
CMTI						
$CMTI_H$	Output High Level Common Mode Transient Immunity	V_I = V_{CC1}, V_{CM}=1200V, C_L=15pF		150		kV/us
$CMTI_L$	Output Low Level Common Mode Transient Immunity	V_I = 0V, V_{CM}=1200V, C_L=15pF		150		kV/us

SWITCHING CHARACTERISTICS (AC) WITH 3.3V SUPPLY

V_{CC1} = V_{CC2}=3.3V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay, Low to High	C_L=15pF		13	25	ns
t_{PHL}	Propagation delay, High to Low	C_L=15pF		13	25	ns
t_r	Turn on rise time	C_L=15pF		2.2		ns
t_f	Turn off fall time	C_L=15pF		2.1		ns
t_{PWD}	Pulse Width Distortion	C_L=15pF			10	ns
t_{SKO}	Channel to Channel Output Skew Time	C_L=15pF, same direction in single device			8	ns
t_{SKP}	Part to Part Skew Time	C_L=15pF, same direction			8	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC1} goes below 1.7V		0.15		us

ELECTRICAL CHARACTERISTICS (DC) WITH 2.5V SUPPLY

V_{CC1} = V_{CC2}=2.5V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
Power Supply UVLO						
$UVLO_R$	Under Voltage Lockout V_{CCx} rising			2.05	2.25	V
$UVLO_F$	Under Voltage Lockout V_{CCx} falling		1.7	1.9		V
$UVLO_{HYS}$	Under Voltage Lockout Hysteresis			0.15		V
Power Supply Current						
I_{CC1_Q}	Current on VCC1 with complementary input	V_{IH} = V_{CC1} ,V_{IL} = 0V or V_{IH} = 0V ,V_{IL} = V_{CC1}		4.3	5.9	mA
I_{CC2_Q}	Current on VCC2 with complementary input			3.2	4.6	mA
$I_{CC1\_OP\_1M}$	Current on VCC1 at 1Mbps	1 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.3	6.5	mA
$I_{CC1\_OP\_10M}$	Current on VCC1 at 10Mbps	10 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.3	6.5	mA
$I_{CC1\_OP\_50M}$	Current on VCC1 at 50Mbps	50 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.5	7.2	mA
$I_{CC1\_OP\_100M}$	Current on VCC1 at 100Mbps	100 Mbps, C_L = 15pF, all channel switching with square wave clock input		4.7	7.5	mA
$I_{CC2\_OP\_1M}$	Current on VCC2 at 1Mbps	1 Mbps, C_L = 15pF, all channel switching with square wave clock input		3.4	5.4	mA
$I_{CC2\_OP\_10M}$	Current on VCC2 at 10Mbps	10 Mbps, C_L = 15pF, all channel switching with square wave clock input		5.3	8.4	mA
$I_{CC2\_OP\_50M}$	Current on VCC2 at 50Mbps	50 Mbps, C_L = 15pF, all channel switching with square wave clock input		13.0	18.5	mA
$I_{CC2\_OP\_100M}$	Current on VCC2 at 100Mbps	100 Mbps, C_L = 15pF, all channel switching with square wave clock input		21.8	30.5	mA
Input Logic Interface						
V_{IH}	Rising input threshold voltage			0.6× V_{CC1}	0.7× V_{CC1}	V

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
V_{IL}	Falling input threshold voltage		0.3× V_{CC1}	0.4× V_{CC1}		V
V_{IHYS}	Input threshold voltage hysteresis			0.2× V_{CC1}		V
I_{IH}	High level input current	V_{INx} = V_{CC1}			10	uA
I_{IL}	Low level input current	V_{INx} = 0V	-10			uA
Output Logic Interface						
V_{OH}	High level output voltage	I_{OH} = -1mA	V_{CC2} -0.2	2.45		V
V_{OL}	Low level output voltage	I_{OL} = 1mA		0.04	0.1	V
CMTI						
$CMTI_H$	Output High Level Common Mode Transient Immunity	V_I = V_{CC1}, V_{CM}=1200V, C_L=15pF		150		kV/us
$CMTI_L$	Output Low Level Common Mode Transient Immunity	V_I = 0V, V_{CM}=1200V, C_L=15pF		150		kV/us

SWITCHING CHARACTERISTICS (AC) WITH 2.5V SUPPLY

V_{CC1} = V_{CC2}=2.5V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay, Low to High	C_L=15pF		14	27	ns
t_{PHL}	Propagation delay, High to Low	C_L=15pF		14	27	ns
t_r	Turn on rise time	C_L=15pF		2.4		ns
t_f	Turn off fall time	C_L=15pF		2.3		ns
t_{PWD}	Pulse Width Distortion	C_L=15pF			10	ns
t_{SKO}	Channel to Channel Output Skew Time	C_L=15pF, same direction in single device			8	ns
t_{SKP}	Part to Part Skew Time	C_L=15pF, same direction			8	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC1} goes below 1.7V		0.15		us

PARAMETER MEASUREMENT INFORMATION

Switching Characteristics Test Timing

Figure 5 shows the timing of propagation delay, rise and fall time

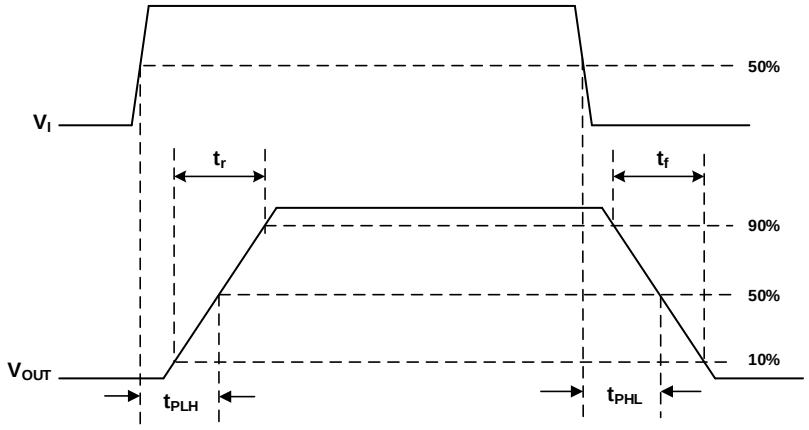
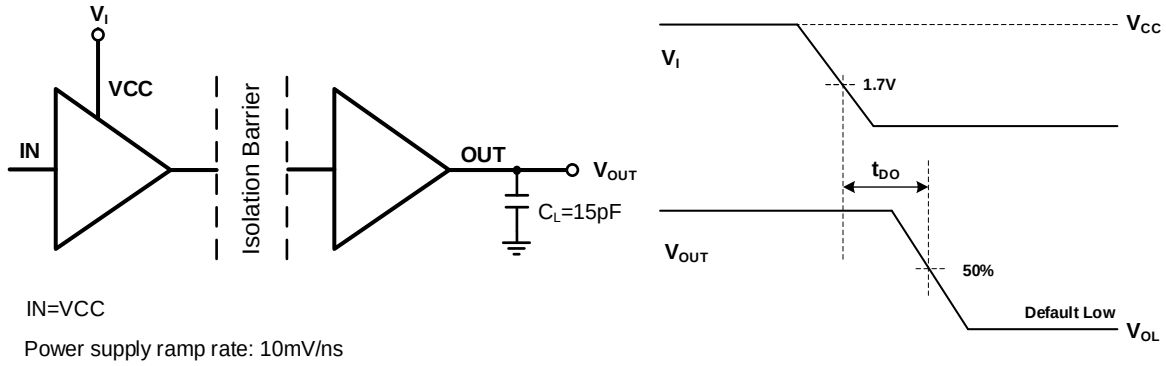


Figure 5. Propagation Delay, Rise Time and Fall Time



IN=VCC

Power supply ramp rate: 10mV/ns

Figure 6. Default Output Delay Time Test

CMTI Testing

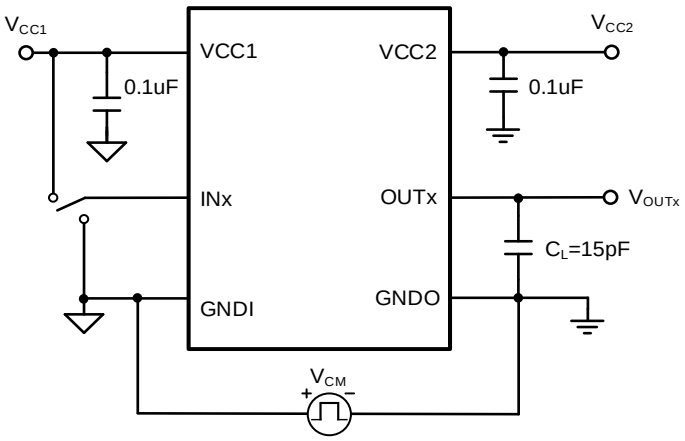


Figure 7. CMTI Test Configuration

FEATURE DESCRIPTION

The SiLM5768L and SiLM5768LN devices are high-performance, six-channel digital isolators with interlock function to enable a variety of application uses. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. The SiLM5768L provides a standard non-inverting channel output and the SiLM5768LN provides inverting channel output. With innovative chip design and layout techniques, the electromagnetic compatibility of the SiLM5768L devices has been significantly enhanced to improve the robustness of overall system.

Interlock Function

The SiLM5768L/SiLM5768LN integrates the interlock function to prevent adjacent channel pairings from both output high simultaneously. This interlock circuitry provides protection preventing shoot through current to both the high side and low-side switch in a bridge circuit. When one of the channel pairings is logic high, the other channel will output logic low. The Table 1 shows the relationship between logic input and output of the SiLM5768L(Non-Inverting output) and the Table 2 shows the relationship between logic input and output of the SiLM5768LN(Inverting output)

Table 1. SiLM5768L Truth Table

INx_H	INx_L	OUTx_H	OUTx_L
High	Low	High	Low
Low	High	Low	High
High	High	Low	Low
Low	Low	Low	Low
Floating	Floating	Low	Low

Table 2. SiLM5768LN Truth Table

INx_H	INx_L	OUTx_H	OUTx_L
High	Low	Low	High
Low	High	High	Low
High	High	Low	Low
Low	Low	Low	Low
Floating	Floating	Low	Low

Device Functional Modes

The Table 3 shows the functional modes of the SiLM5768L/SiLM5768LN.
Table 3. Function Table

V_{CC1}	V_{CC2}	Input (INx_H and INx_L)	Output (OUTx_H and OUTx_L)	Function Description
PU(1)	PU	H	Normal	Normal operation. The output is controlled by the input as shown in the Table 1. SiLM5768L Truth Table and Table 2. SiLM5768LN Truth Table
		L		
		Open		
PD(1)	PU	X	Low	Output low: When V_{CC1} is unpowered and V_{CC2} is powered up, the output interlock circuit will set the output to logic low.
X(1)	PD	X	Undetermined(2)	When V_{CC2} is unpowered, channel output is undermined.

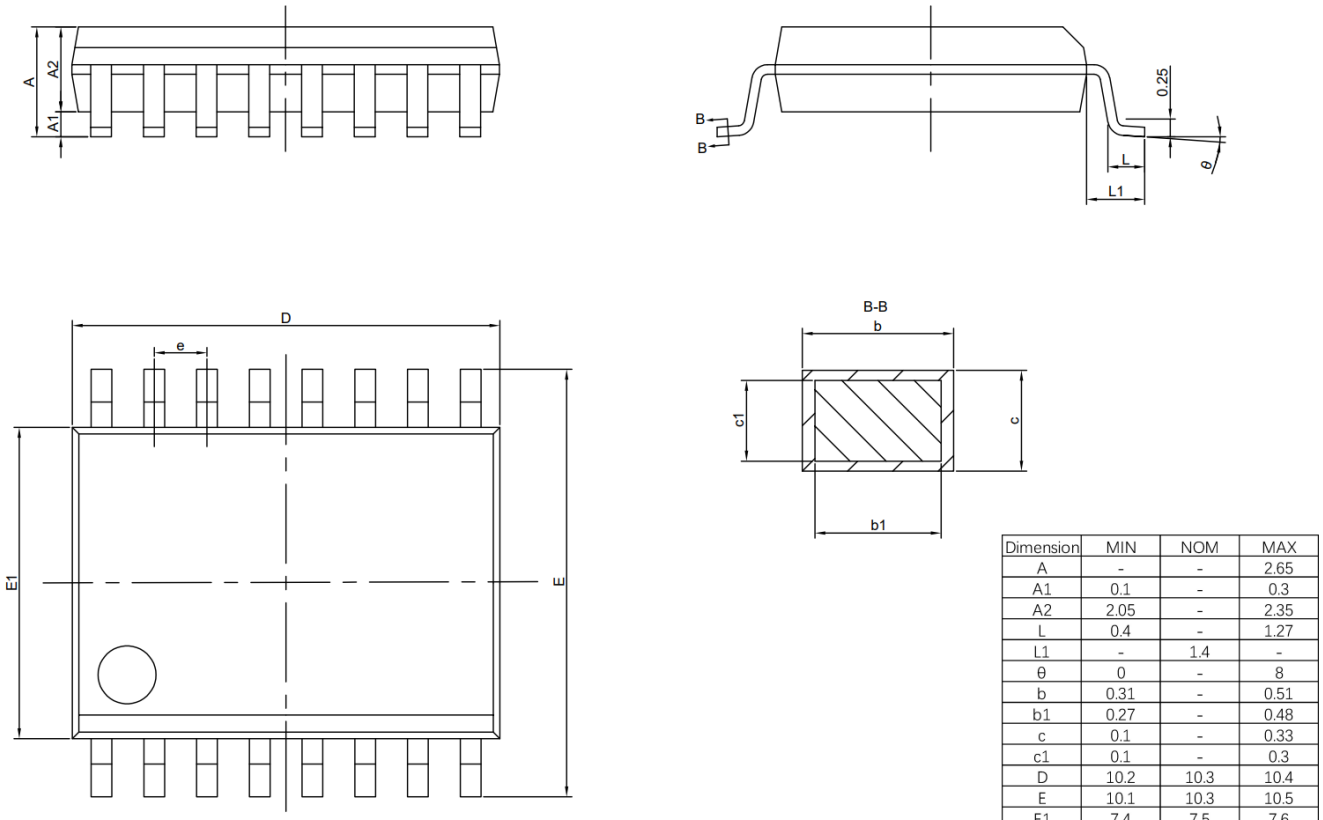
(1) PU=Powered up, $V_{CC} \geqslant 2.25V$; PD=Powered down, $V_{CC} \leqslant 1.7V$; X=Irrelevant

(2) The outputs are in undermined state when $1.7 < V_{CC1}, V_{CC2} < 2.25V$

Power Supply Recommendation

A 0.1μF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}) to help ensure reliable operation. The capacitors should be placed as close to the supply pins as possible.

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	2.65
A1	0.1	-	0.3
A2	2.05	-	2.35
L	0.4	-	1.27
L1	-	1.4	-
θ	0	-	8
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.1	-	0.33
c1	0.1	-	0.3
D	10.2	10.3	10.4
E	10.1	10.3	10.5
E1	7.4	7.5	7.6
e	1.02	1.27	1.52
Unit : mm			

Figure 8. SOP16W Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: 2024-06-11	
Whole document	Initial datasheet release