600V Half Bridge Driver

PRODUCT SUMMARY

- **V_{OFFSET}** 600 V max.
- **I_O+/- (typ.)** 290 mA/600 mA
- **V_{OUT}** 10 V - 22 V
- **$t_{on/off}$ (typ.)** 200 ns/200 ns
- **Deadtime** 220 ns

GENERAL DESCRIPTION

The SiLM2234 is a high voltage, high speed power MOSFET and IGBT drivers. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to 600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 22 V
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Maximum negative input voltage handling on input -5V
- Integrate boost diode
- Matched propagation delay for both channels
- UVLO for both high-side and low-side drivers
- Outputs in phase with inputs
- RoHS compliant
- SOP8 package

TYPICAL APPLICATION CIRCUIT

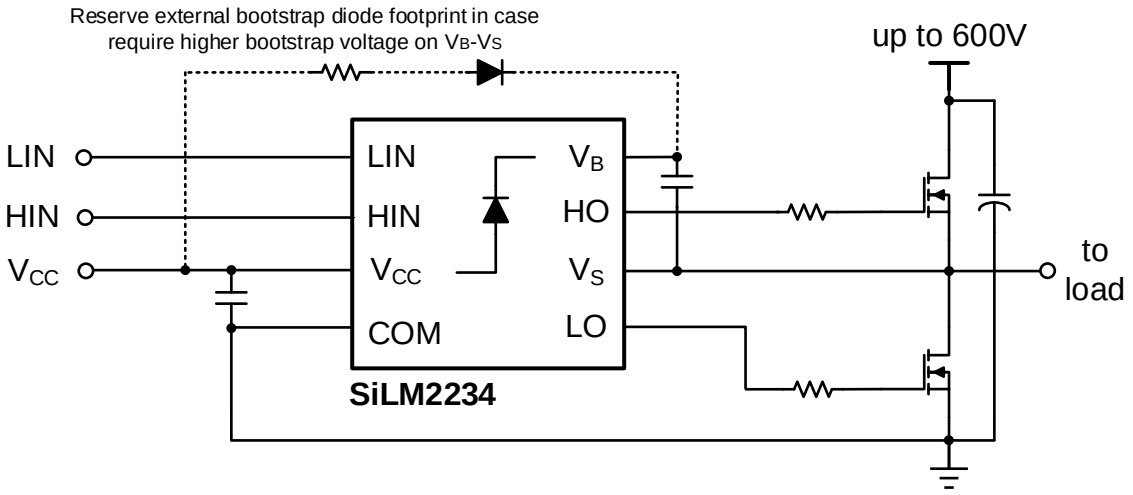

Figure 1. Typical Application Circuit

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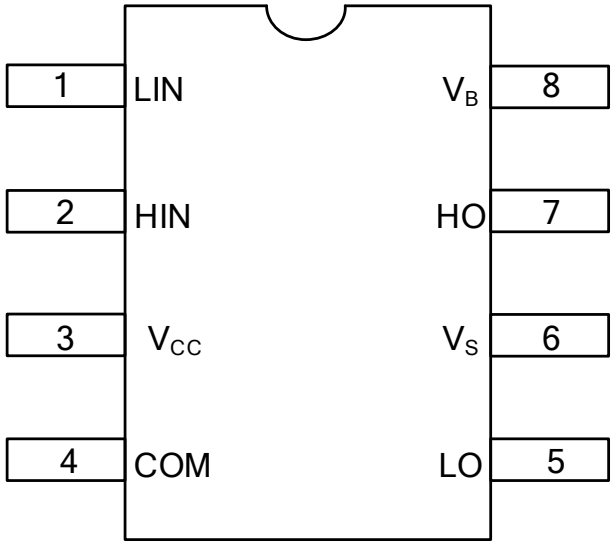
PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP8	

PIN DESCRIPTION

No.	Pin	Description
1	LIN	Logic input for low-side gate driver output (LO), in phase
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	V_{CC}	Low-side and logic fixed supply
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V_S	High-side floating supply return
7	HO	High-side gate drive output
8	V_B	High-side floating supply

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SiLM2234CA-DG	SOP8, Pb-Free	2500/Reel

FUNCTIONAL BLOCK DIAGRAM

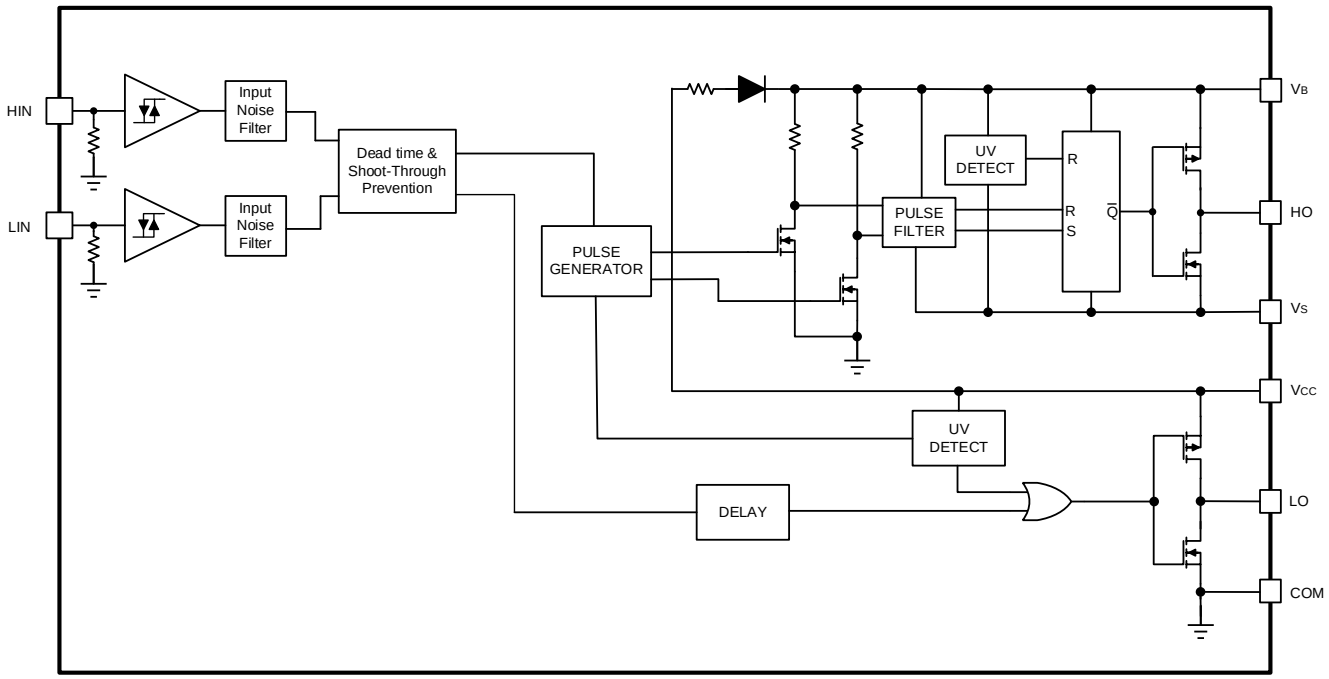


Figure 2. Function Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	- 0.3	625	V
V_S	High-side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage	- 0.3	25	
V_{LO}	Low-side output voltage	- 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)	- 6	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient	---	50	V/ns
P_D	Package power dissipation @ $T_A \leqslant$ +25°C	---	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	---	200	°C/W
T_J	Junction temperature	---	150	°C
T_S	Storage temperature	- 55	150	
T_L	Lead temperature (soldering, 10 seconds)	---	300	

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	V_S + 10	V_S + 22	V
V_S	High-side floating supply offset voltage	- 9	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	22	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN)	- 5	V_{CC}	
T_A	Ambient temperature	- 40	125	°C

Note: The input/output logic timing diagram is shown in Figure 3. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S = 0 V	---	200	260	ns
t_{off}	Turn-off propagation delay	V_S = 0 V	---	200	260	
t_r	Turn-on rise time		---	70	120	
t_f	Turn-off fall time		---	25	60	
DT	Deadtime		100	220	360	
MT	Delay matching, HS & LS turn-on/off		---	---	50	

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM and are applicable to all logic input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic “1” input voltage threshold		1.6	2.0	2.4	V
V_{IL}	Logic “0” input voltage threshold		0.8	1.1	1.5	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2 mA	---	0.05	0.2	
V_{OL}	Low level output voltage, V_O		---	0.02	0.1	
I_{LK}	Offset supply leakage current	V_B = V_S = 600 V	---	---	50	µA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V	---	60	80	
I_{QCC}	Quiescent V_{CC} supply current		---	180	300	
I_{IN+}	Logic “1” input bias current	V_{IN} = 5V	---	8	20	
I_{IN-}	Logic “0” input bias current	V_{IN} = 0V	---	---	5	
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold		8	8.9	9.8	V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold		7.4	8.2	9	
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold		7	7.9	8.8	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold		6.4	7.2	8	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{O+}	Output high short circuit pulsed current[1]	V_O = 0V, V_{IN} =Logic “1”, PW ≤ 10 μs	130	290	---	mA
I_{O-}	Output low short circuit pulsed current[1]	V_O =15V, V_{IN}=Logic “0”, PW ≤ 10 μs	270	600	---	
V_{F_BSD}	Forward voltage drop from V_{CC} to V_B	I_F=1mA	---	1.9	2.8	V
R_{BSD}	Bootstrap diode on resistor		---	350	---	Ω

1）Bench characterization.

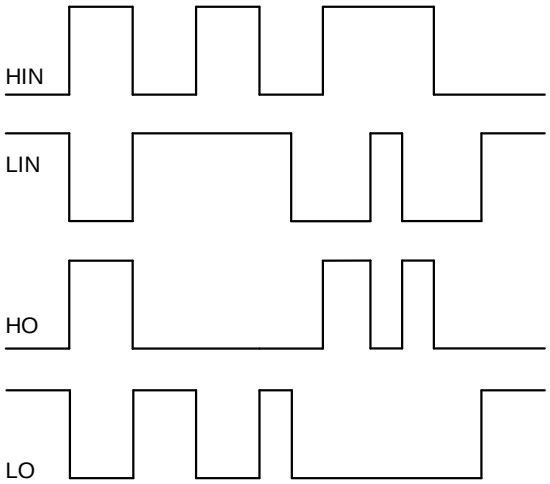


Figure 3. Input/Output Timing Diagram

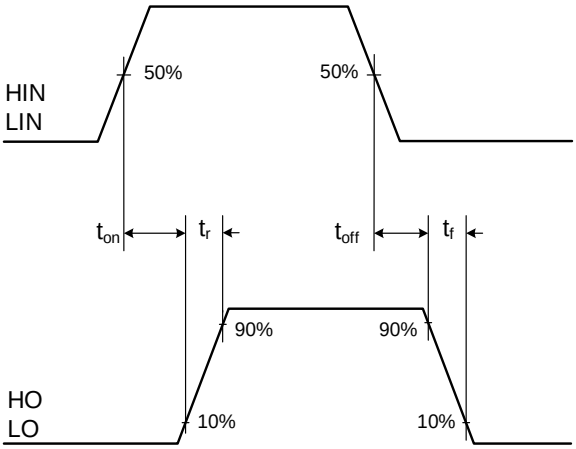


Figure 4. Switching Time Waveform

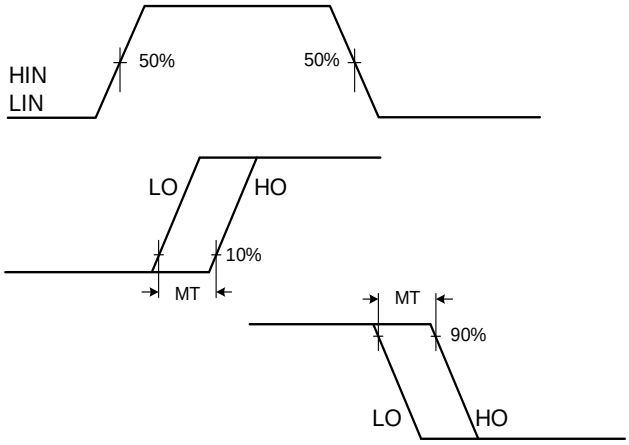


Figure 5. Delay Matching Waveform

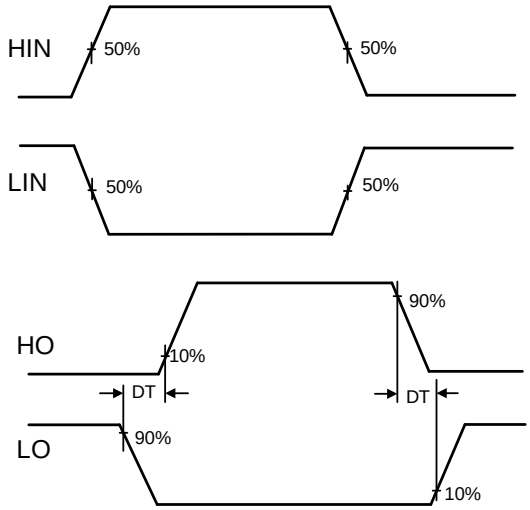
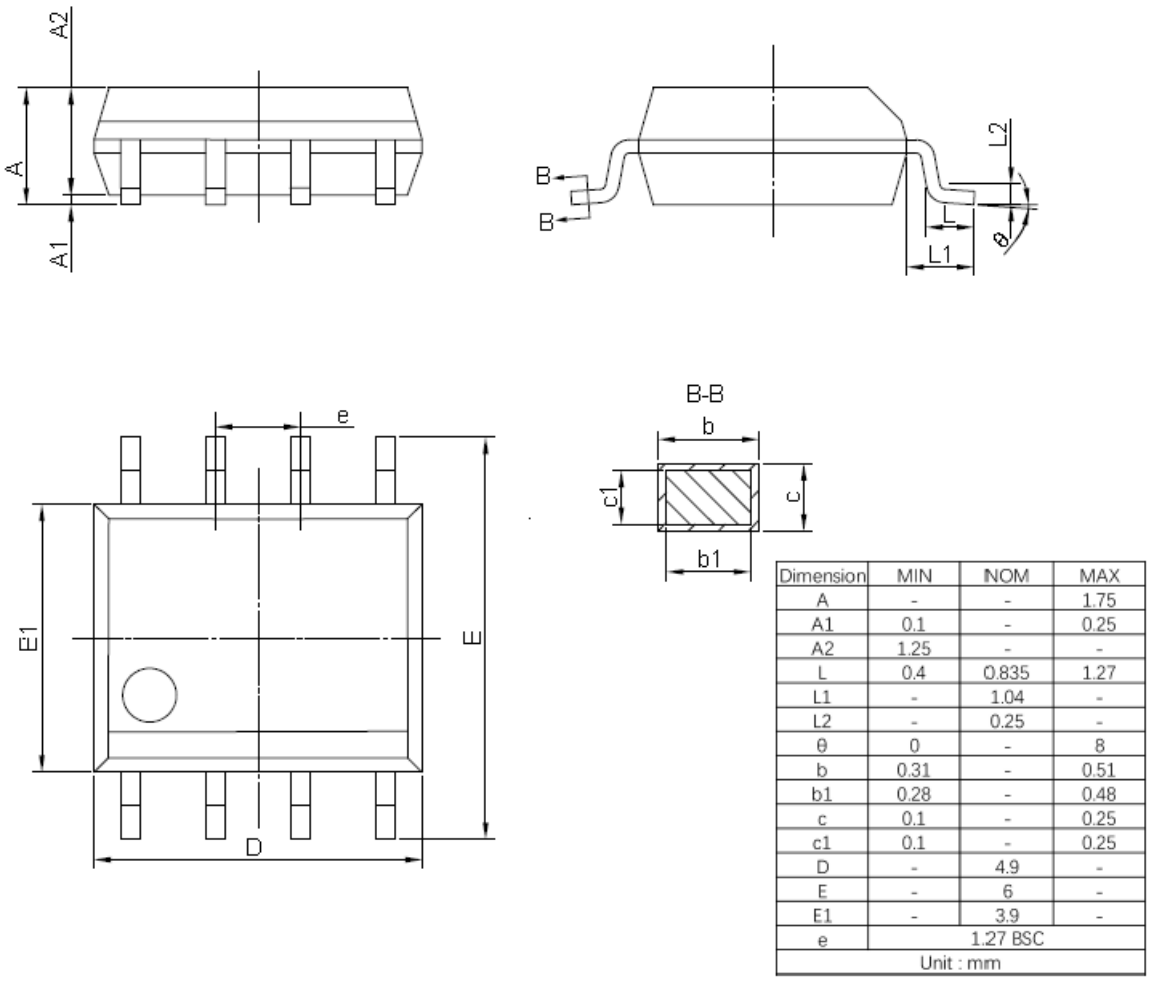


Figure 6. Dead Time Waveform

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
L2	-	0.25	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	-	4.9	-
E	-	6	-
E1	-	3.9	-
e	1.27 BSC		
Unit : mm			

Figure 7. SOP8 Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 Datasheet, 2025-11-28	
Whole datasheet	Initial datasheet release