Fault Protected CAN Transceiver with CAN FD

GENERAL DESCRIPTION

The SiLM104x/5xS is a high speed controller area network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 high speed CAN specification. The SiLM104x/5xS transceiver supports both classical CAN and CAN FD (Flexible Data Rate) networks up to 5 megabits per second (Mbps). The SiLM104x/5xS includes internal logic level translation via the V_{IO} terminal to allow for interfacing the transceiver IOs directly to 1.8V, 2.5V, 3.3V, or 5V logic IOs. The transceiver has a low power standby mode which supports remote wake up via the ISO 11898-2:2016 defined wake-up pattern (WUP). The SiLM104x/5xS transceiver also includes many protections and diagnostic features including thermal-shutdown (TSD), TXD-dominant time-out (DTO), supply undervoltage detection, and bus fault protection up to ±65 V.

APPLICATION

- All devices support highly loaded CAN networks
- Industrial Automation, Control, Sensors and Drive Systems
- Building, Security and Climate Control Automation
- Telecom Base Station Status and Control

FEATURES

- Meets the requirements of ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards
- Support of classical CAN and optimized CAN FD performance at 2, 5 Mbps
- IO voltage range supports 1.7 V to 5.5 V
- Receiver common mode input voltage in normal mode: ±30 V
- Receiver common mode input voltage in standby mode: ±12 V
- Protection features
  - Bus fault protection: ±65 V
  - Under-voltage protection
  - TXD-dominant time-out (DTO)
  - Thermal-shutdown protection (TSD)
- Optimized behavior when unpowered
  - Bus and logic pins are high impedance (no load)
  - Hot-plug capable: power up/down with glitch free operation on bus and RXD output

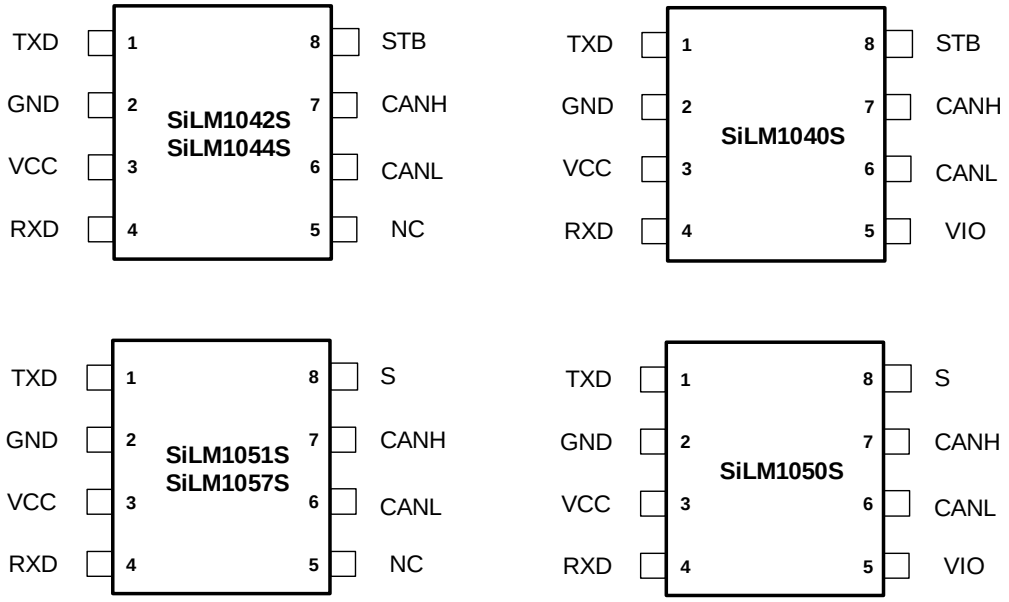

Figure 1. SiLM104x/5xS

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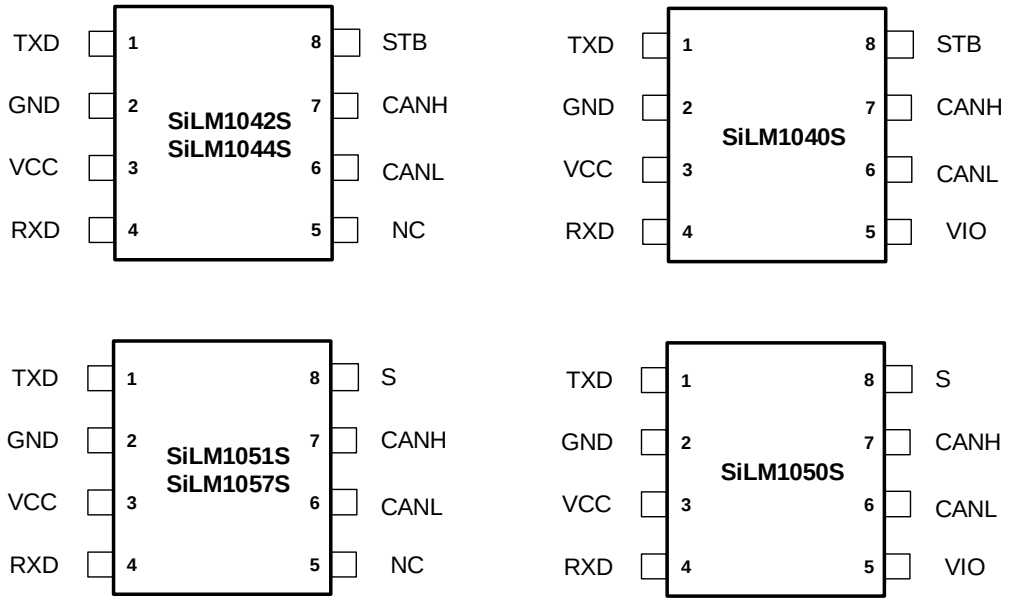
PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP8	

PIN DESCRIPTION

No.	Pin Name	Description
1	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	GND	Ground
3	VCC	Transceiver 5V supply voltage
4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	NC	Not Connection in SiLM1042S, SiLM1044S, SiLM1051S and SiLM1057S
	VIO	Transceiver I/O level shifting supply voltage in SiLM1040S and SiLM1050S
6	CANL	Low level CAN bus input/output line
7	CANH	High level CAN bus input/output line
8	STB	Standby Mode control input in SiLM1040S, SiLM1042S and SiLM1044S. The part enters standby mode if the STB is pulled high. The part works in normal mode when STB is pulled low.
	S	Silent Mode control input in SiLM1050S, SiLM1051S and SiLM1057S. The part enters silent mode if the S pin is pulled high. The part works in normal mode when S pin is pulled low.

FUNCTIONAL BLOCK DIAGRAM

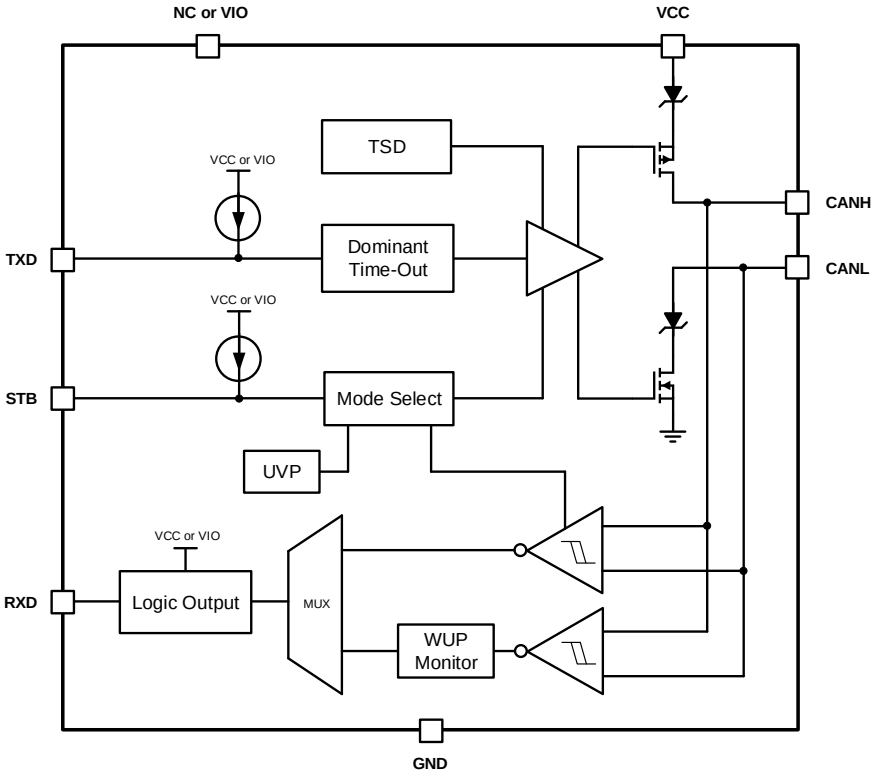


Figure 2. SiLM1040/42/44S Block Diagram

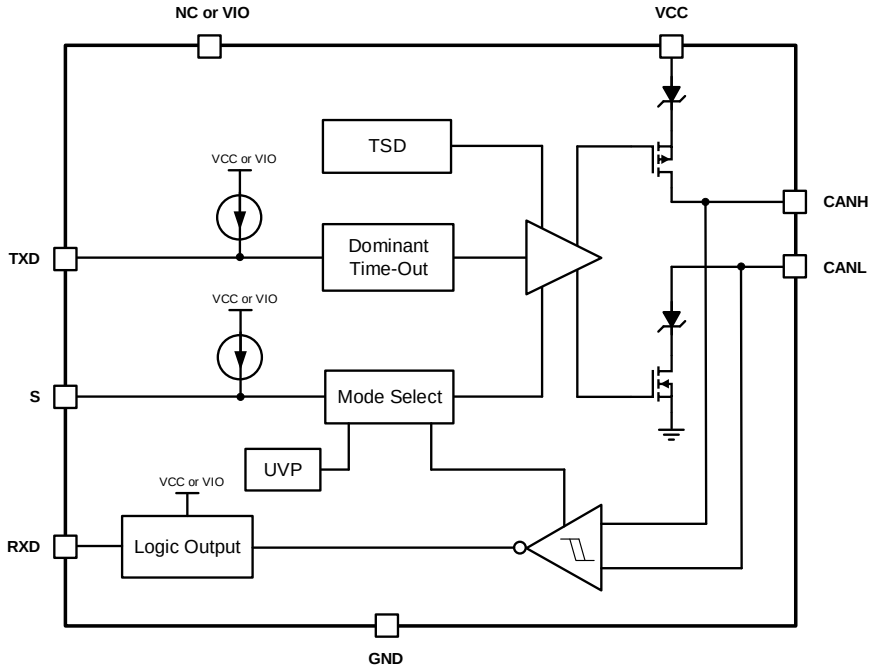


Figure 3. SiLM1050/51/57S Block Diagram

ORDERING INFORMATION

Order Part No.	Package	QTY
SiLM1040SCA-DG	SOP8, Pb-Free	2500/Reel
SiLM1042SCA-DG	SOP8, Pb-Free	2500/Reel
SiLM1044SCA-DG	SOP8, Pb-Free	2500/Reel
SiLM1050SCA-DG	SOP8, Pb-Free	2500/Reel
SiLM1051SCA-DG	SOP8, Pb-Free	2500/Reel
SiLM1057SCA-DG	SOP8, Pb-Free	2500/Reel

FAMILY OVERVIEW

Part Number	With VIO Pin	Standby or Silent Mode	Input IO Logic Level
SiLM1040S	Yes	Standby	CMOS
SiLM1042S	No	Standby	TTL
SiLM1044S	No	Standby	CMOS
SiLM1050S	Yes	Silent	CMOS
SiLM1051S	No	Silent	TTL
SiLM1057S	No	Silent	CMOS

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Units
V_{CC}	Supply Voltage	-0.3	6	V
V_{IO}	IO Level Shifting Voltage	-0.3	6	V
V_{BUS}	CANH, CANL Voltage	-65	65	V
V_{DIFF}	Max differential voltage between CANH and CANL	-65	65	V
V_I	Logic input voltage TXD, STB, S	-0.3	6 and $V_I \leqslant V_{IO}+0.3$	V
V_O	Logic output voltage RXD	-0.3	6 and $V_I \leqslant V_{IO}+0.3$	V
I_{RXD}	RXD output current	-8	8	mA
T_J	Junction Temperature	-55	150	°C
T_S	Storage Temperature	-65	150	

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min	Max	Units
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IO}	IO Level Shifting Voltage	1.7	5.5	V
I_{RXD}	RXD output current	-2	2	mA
T_A	Ambient Temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM All Terminals	±4000	V
	HBM CANH and CANL to GND	±8000	
	CDM	±1500	
	System level ESD, IEC61000-4-2: Powered contact discharge: CANH and CANL to GND	±6000	

ELECTRICAL CHARACTERISTICS (DC)

All typical values at V_{CC} = 5V, V_{IO} = 5V and T_A = 25°C, all min and max specifications are at recommended operating conditions and T_A = -40°C to 125°C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Characteristics						
I_{CC1}	VCC Current, Normal mode (dominant)	R_L=60Ω, STB/S=GND, TXD=GND		47	75	mA
I_{CC2}		R_L=50Ω, STB/S=GND, TXD=GND		52	80	mA
I_{CC3}	VCC Current, Normal mode (recessive)	R_L=50Ω, STB/S=GND, TXD=VCC or VIO		0.4	1	mA
I_{CC4}	VCC Current, Normal mode (bus fault)	CANH = CANL = +/- 25V, STB/S=GND, R_L=open			125	mA
I_{CC5}	VCC Current, Standby Mode without VIO	R_L=50Ω, STB=VCC, TXD=VCC		22	30	uA
I_{CC6}	VCC Current, Standby Mode with VIO	R_L=50Ω, STB=TXD=VIO=5V		0.6	5	uA
I_{CC7}	VCC Current, Silent Mode without VIO	R_L=50Ω, S=VCC, TXD=VCC		0.4	1	mA
I_{CC8}	VCC Current, Silent Mode with VIO	R_L=50Ω, S=TXD=VIO=5V		0.4	1	mA
I_{IO1}	VIO Current, Normal Mode (dominant)	STB/S=GND, TXD=GND		45	150	uA
I_{IO2}	VIO Current, Normal Mode (recessive)	STB/S=GND, TXD=VIO		18	50	uA
I_{IO3}	VIO Current, Silent Mode	TXD=S=VIO		6.8	15	uA
I_{IO4}	VIO Current, Standby Mode	TXD=STB=VIO		12.6	20	uA
$V_{UV\_VCC\_R}$	Under Voltage Lockout Rising on VCC		4	4.2	4.4	V
$V_{UV\_VCC\_F}$	Under Voltage Lockout Falling on VCC		3.8	4	4.2	V
$V_{UV\_VCC\_HYS}$	Under Voltage Lockout Hysteresis on VCC			0.2		V
$V_{UV\_VIO\_R}$	Under Voltage Protection Threshold Voltage on VIO, Rising		1.3	1.45	1.7	V
$V_{UV\_VIO\_HYS}$	Under Voltage Protection Hysteresis Voltage on VIO			30		mV
T_{TSD}	Thermal Shutdown Temperature			190		°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{TSD_HYS}	Thermal Shutdown Hysteresis			15		°C
Driver Characteristics						
$V_{OCANH(DOM)}$	CANH Bus Output Voltage, Dominant	50Ω ≤ R_L ≤ 65Ω, TXD=0V	2.75		4.5	V
$V_{OCANL(DOM)}$	CANL Bus Output Voltage, Dominant	50Ω ≤ R_L ≤ 65Ω, TXD=0V	0.5		2.25	V
$V_{OCANH(REC)}$	CANH Bus Output Voltage, Recessive	R_L=Open, TXD=V_{CC}	2	0.5 x V_{CC}	3	V
$V_{OCANL(REC)}$	CANL Bus Output Voltage, Recessive	R_L=Open, TXD=V_{CC}	2	0.5 x V_{CC}	3	V
$V_{OCANH(STB)}$	CANH Bus Output Voltage, Standby	R_L=Open	-0.1		0.1	V
$V_{OCANL(STB)}$	CANL Bus Output Voltage, Standby	R_L=Open	-0.1		0.1	V
$V_{OCAN(STB)}$	CANH-CANL Bus Output Voltage, Standby	R_L=Open	-0.2		0.2	V
$V_{OD(DOM)}$	Differential Output Voltage, Dominant	50Ω ≤ R_L ≤ 65Ω, TXD=0V	1.5		3.0	V
$V_{OD(REC)}$	Differential Output Voltage, Recessive	R_L=Open, TXD=V_{CC}	-50		50	mV
V_{SYM}	Output Symmetry (Dominant or Recessive), (V_{OCANH} + V_{OCANL}) / V_{CC}	50Ω ≤ R_L ≤ 65Ω, TXD=V_{CC} or 0V	0.9		1.1	V/V
V_{SYM_DC}	DC Output Symmetry (Dominant or Recessive), V_{CC} - (V_{OCANH} + V_{OCANL})	50Ω ≤ R_L ≤ 65Ω, TXD=V_{CC} or 0V	-0.4		0.4	V
I_{OSCH_DOM}	CANH Output Short Circuit Current, Dominant Normal Mode	CANH=-15V to 40V, CANL Open, TXD=0V	-115			mA
I_{OSCL_DOM}	CANL Output Short Circuit Current, Dominant Normal Mode	CANL=-15V to 40V, CANH Open, TXD=0V			115	mA
I_{OSC_REC}	Output Short Circuit Current, Recessive Normal Mode	CANH=CANL=-40V to 40V, TXD= V_{CC}	-5		5	mA
Logic IOs						
V_{IH}	Input High Threshold (TXD, STB, S) without VIO (SiLM1042S, SiLM1051S)		2			V
V_{IL}	Input Low Threshold (TXD, STB, S) without VIO (SiLM1042S, SiLM1051S)				0.8	V
V_{IH}	Input High Threshold (TXD, STB, S) without VIO (SiLM1044S, SiLM1057S)		70%			V_{CC}

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Threshold (TXD, STB, S) without VIO (SiLM1044S, SiLM1057S)				30%	V_{CC}
V_{IH}	Input High Threshold (TXD, STB, S) with VIO (SiLM1040S, SiLM1050S)		70%			V_{IO}
V_{IL}	Input Low Threshold (TXD, STB, S) with VIO (SiLM1040S, SiLM1050S)				30%	V_{IO}
I_{IH}	High Level Input Leakage (STB, S)	STB or S = VCC = VIO = 5.5V	-2		2	uA
I_{IL}	Low Level Input Leakage (STB, S)	STB or S = 0, VCC = VIO = 5.5V	-20		-2	uA
$I_{LKG(OFF)}$	Unpowered Leakage Current (STB, S)	STB or S = 5.5V, VCC = VIO = 0V	-1		1	uA
I_{IH}	High Level Input Leakage (TXD)	TXD = VCC = VIO = 5.5V	-2.5		1	uA
I_{IL}	Low Level Input Leakage (TXD)	TXD = 0, VCC = VIO = 5.5V	-100		-7	uA
$I_{LKG(OFF)}$	Unpowered Leakage Current (TXD)	TXD = 5.5V, VCC = VIO = 0V	-1		1	uA
V_{OH}	High Level Output Voltage (RXD) with VIO	I_{RXD} = -2mA	80%			V_{IO}
V_{OL}	Low Level Output Voltage (RXD) with VIO	I_{RXD} = 2mA			20%	V_{IO}
V_{OH}	High Level Output Voltage (RXD) without VIO	I_{RXD} = -2mA, V_{CC} = 5V	4.5	4.85		V
V_{OL}	Low Level Output Voltage (RXD) without VIO	I_{RXD} = 2mA, V_{CC} = 5V		0.2	0.5	V
$I_{LKG(OFF)}$	Unpowered Leakage Current (RXD)	RXD = 5.5V, VCC = VIO = 0V	-1		1	uA
$I_{LKG(OFF)}$	Unpowered Leakage Current (CANH, CANL)	CANH = CANL = 5.5V, VCC = VIO = 0V			5	uA
Receiver Characteristics						
V_{CM1}	Common Mode Range, Normal Mode		-30		30	V
V_{CM2}	Common Mode Range, Standby Mode		-12		12	V
V_{IT+}	Positive Going Input Threshold Voltage, Normal Mode	-30V<V_{CM}<30V			0.9	V
V_{IT-}	Negative Going Input Threshold Voltage, Normal Mode	-30V<V_{CM}<30V	0.5			V
V_{IT_HYS}	Hysteresis for Input Threshold Voltage, Normal Mode	-30V<V_{CM}<30V		0.1		V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IT+}	Positive Going Input Threshold Voltage, Standby Mode	-12V<V_{CM}<12V			1.15	V
V_{IT-}	Negative Going Input Threshold Voltage, Standby Mode	-12V<V_{CM}<12V	0.4			V
V_{IT_HYS}	Hysteresis for Input Threshold Voltage, Standby Mode	-12V<V_{CM}<12V		0.1		V
R_{ID}	Differential Input Resistance		50		80	kΩ
R_{IN}	Input Resistance (CANH or CANL)		25		40	kΩ
$R_{IN(M)}$	Input Resistance Matching 1- $R_{IN(CANH)}$/ $R_{IN(CANL)}$		-1		1	%

SWITCHING CHARACTERISTICS (AC)

All typical values at V_{CC} = 5V, V_{IO} = 5V and T_A = 25°C, all min and max specifications are at recommended operating conditions and T_A = -40°C to 125°C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{PROP(LOOP1)}$	Total loop delay, driver input TXD to receiver output RXD, recessive to dominant	R_L=60Ω, C_L=100pF, C_{L_RXD}=15pF, V_{IO}=2.8V to 5.5V	45		180	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input TXD to receiver output RXD, dominant to recessive		70		180	ns
$t_{PROP(LOOP1)}$	Total loop delay, driver input TXD to receiver output RXD, recessive to dominant	R_L=60Ω, C_L=100pF, C_{L_RXD}=15pF, V_{IO}=1.7V	55		200	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input TXD to receiver output RXD, dominant to recessive		75		200	ns
t_{MODE}	Mode change time from Normal to Standby or from Standby to Normal				40	us
t_{WK_FILTER}	Filter time for valid wake up pattern		0.5		1.8	us
$t_{WK\_TIMEOUT}$	Bus wake up timeout		1	2.6	4	ms
t_{PHR}	Driver propagation delay time, high TXD to driver recessive, dominant to recessive	R_L=60Ω, C_L=100pF	25		75	ns
t_{PLD}	Driver propagation delay time, low TXD to driver dominant, recessive to dominant	R_L=60Ω, C_L=100pF	20		80	ns
t_{SKP}	Pulse skew ($\lvert t_{PHR} - t_{PLD} \rvert$)	R_L=60Ω, C_L=100pF			35	ns
t_R	Differential output signal rise time	R_L=60Ω, C_L=100pF	20	36	65	ns
t_F	Differential output signal fall time	R_L=60Ω, C_L=100pF	20	27	60	ns

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{TXD_DTO}	Dominant timeout	R_L=60Ω, C_L=100pF	1.2	2.5	3.8	ms
t_{PRH}	Receiver propagation delay time, driver recessive to RXD high, dominant to recessive	C_{L_RXD}=15pF, V_{IO}=2.8V to 5.5V	40		110	ns
t_{PDL}	Receiver propagation delay time, driver dominant to RXD low, recessive to dominant		30		90	ns
t_{R_RXD}	RXD output signal rise time		3		20	ns
t_{F_RXD}	RXD output signal fall time		3		20	ns
t_{PRH}	Receiver propagation delay time, driver recessive to RXD high, dominant to recessive	C_{L_RXD}=15pF, V_{IO}=1.7V	40		130	ns
t_{PDL}	Receiver propagation delay time, driver dominant to RXD low, recessive to dominant		30		100	ns
t_{R_RXD}	RXD output signal rise time		10		30	ns
t_{F_RXD}	RXD output signal fall time		10		30	ns
$t_{BIT(BUS)}$	Bit time on CAN bus output with $t_{BIT(TXD)}$ = 500ns	R_L=60Ω, C_L=100pF, C_{L_RXD}=15pF, Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$, V_{IO}=2.8V to 5.5V	435		530	ns
	Bit time on CAN bus output with $t_{BIT(TXD)}$ = 200ns		155		210	ns
$t_{BIT(RXD)}$	Bit time on RXD output with $t_{BIT(TXD)}$ = 500ns		400		550	ns
	Bit time on RXD output with $t_{BIT(TXD)}$ = 200ns		120		220	ns
Δt_{REC}	Receiver timing Symmetry $t_{BIT(TXD)}$ = 500ns		-65		40	ns
	Receiver timing Symmetry $t_{BIT(TXD)}$ = 200ns		-45		15	ns
$t_{BIT(BUS)}$	Bit time on CAN bus output with $t_{BIT(TXD)}$ = 500ns	R_L=60Ω, C_L=100pF, C_{L_RXD}=15pF, Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$, V_{IO}=1.7V	460		600	ns
	Bit time on CAN bus output with $t_{BIT(TXD)}$ = 200ns		170		230	ns
$t_{BIT(RXD)}$	Bit time on RXD output with $t_{BIT(TXD)}$ = 500ns		440		580	ns
	Bit time on RXD output with $t_{BIT(TXD)}$ = 200ns		130		230	ns
Δt_{REC}	Receiver timing Symmetry $t_{BIT(TXD)}$ = 500ns		-65		45	ns
Δt_{REC}	Receiver timing Symmetry $t_{BIT(TXD)}$ = 200ns		-45		20	ns

PARAMETER MEASUREMENT INFORMATION

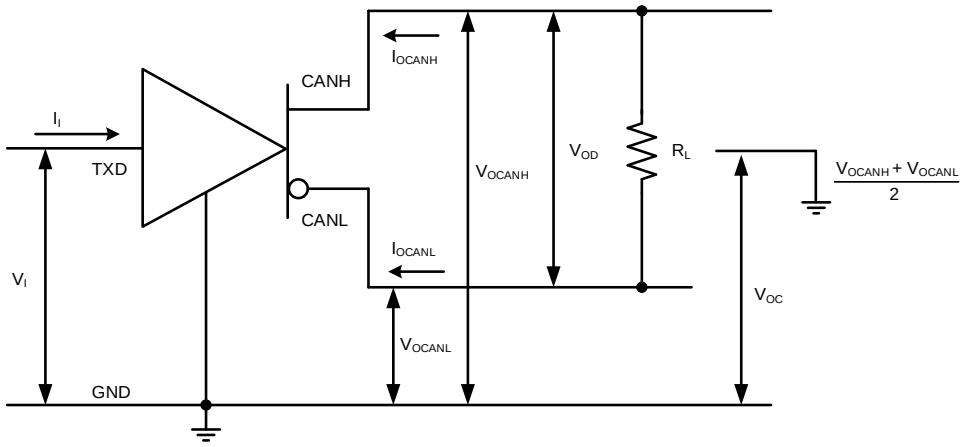


Figure 4. Driver Voltage and Current

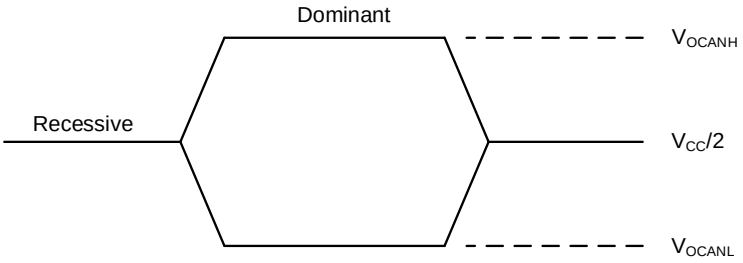


Figure 5. Bus Logic State Voltage Definition

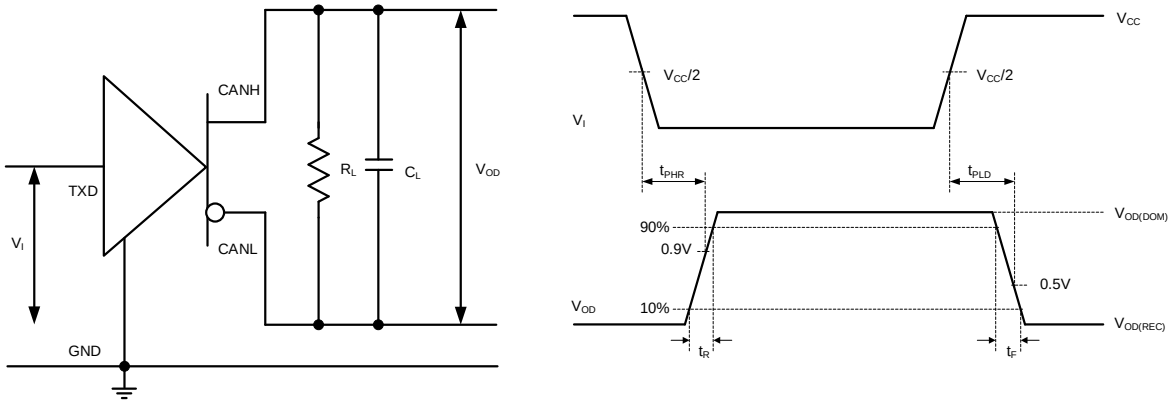


Figure 6. Driver Test Circuit and Timing

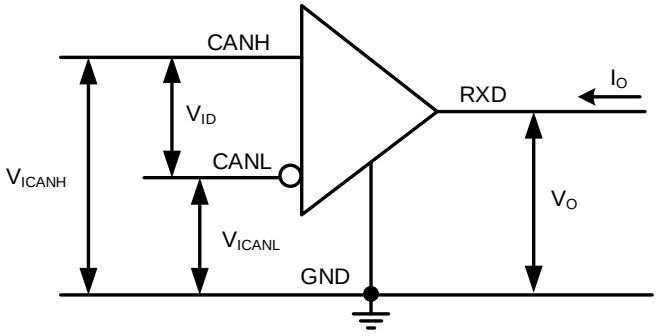


Figure 7. Receiver Voltage and Current

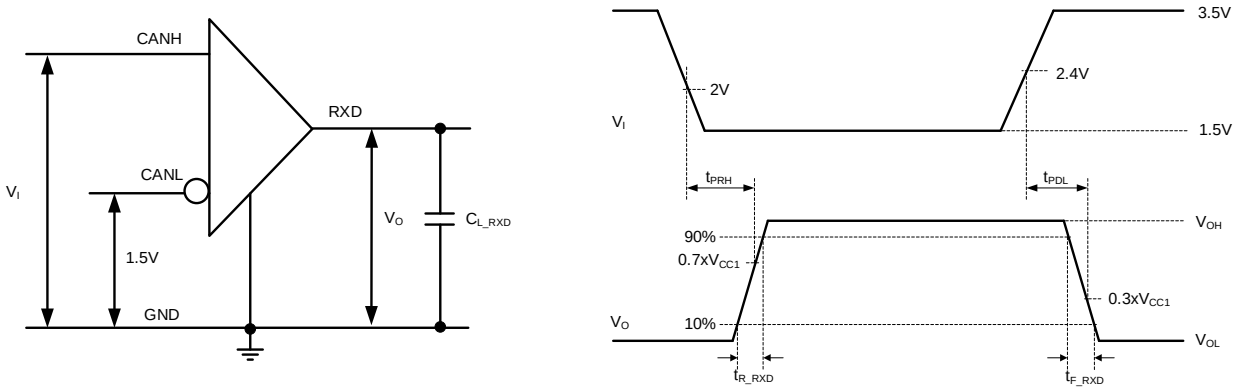


Figure 8. Receiver Test Circuit and Timing

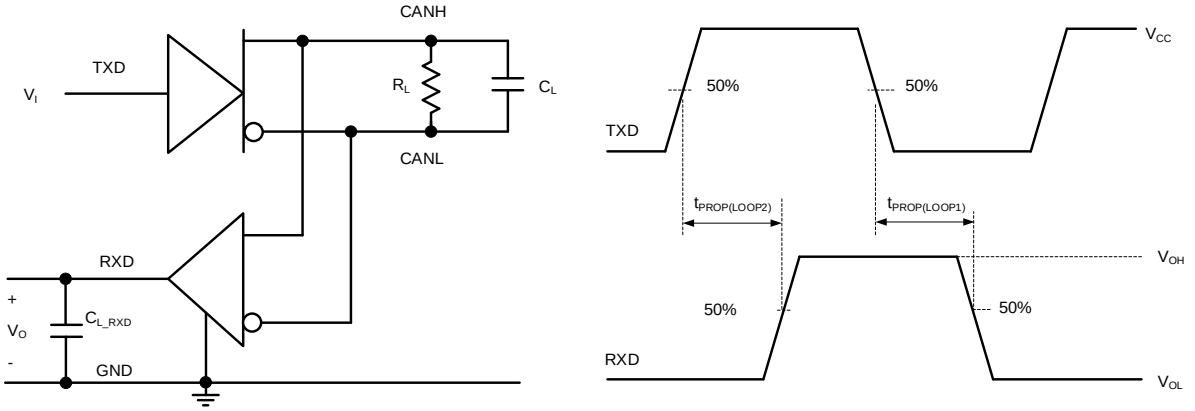


Figure 9. t_{LOOP} Test Circuit and Timing

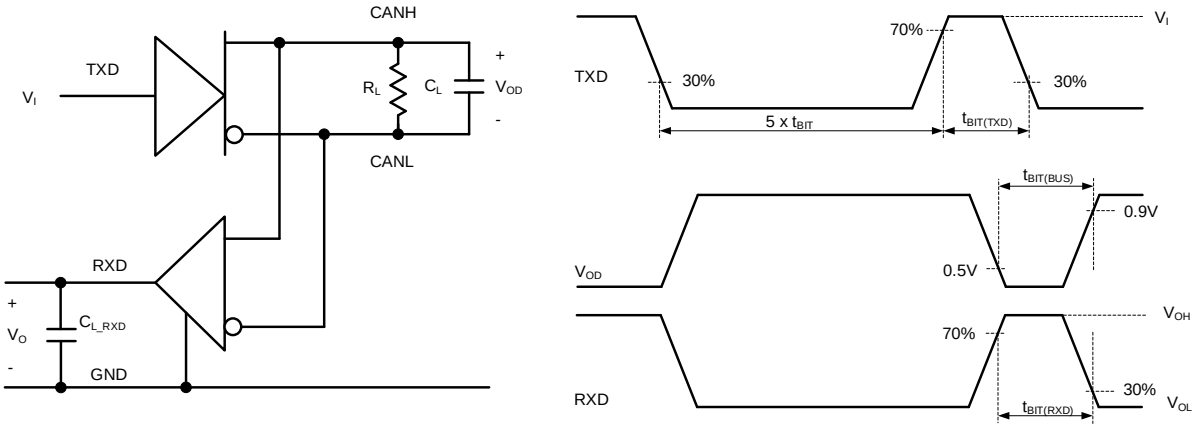


Figure 10. CAN FD Test Circuit and Timing

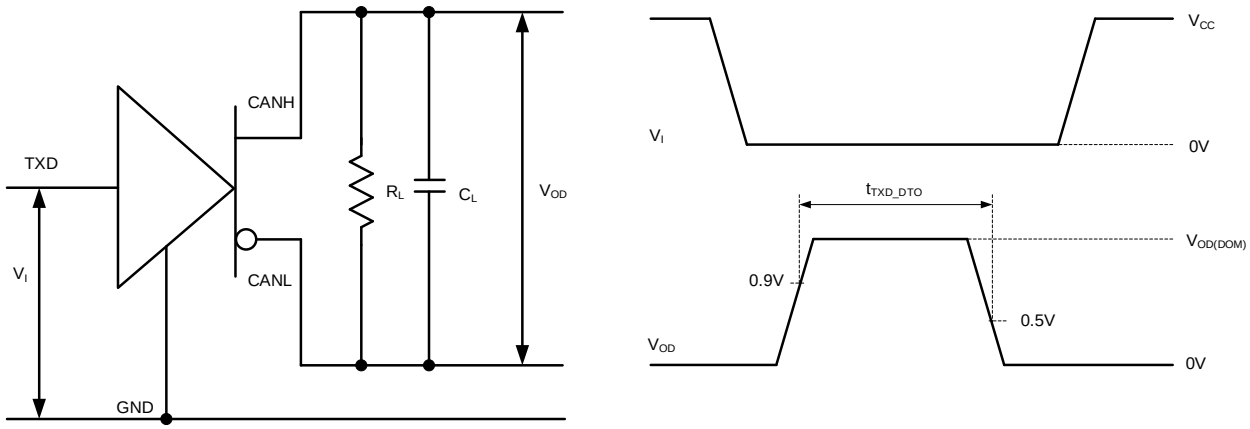


Figure 11. Dominant Time-Out Test Circuit and Timing

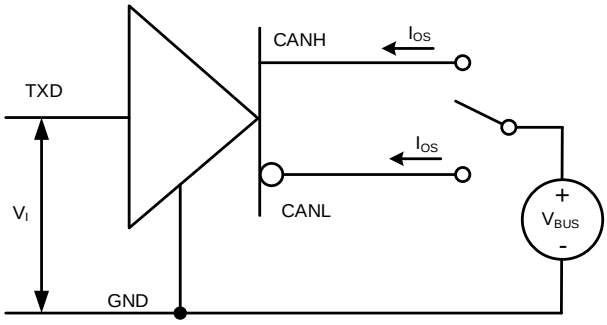


Figure 12. Driver Short Circuit Current Test Circuit

FEATURE DESCRIPTION

The SiLM104x/5xS meets or exceeds the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. They are designed for data rates in excess of 1 Mbps for CAN FD and enhanced timing margin or higher data rates in long and highly loaded networks. The transceiver provides a number of different protection features making it ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 5 Mbps.

CAN Bus State

The CAN bus has two logical states during operation: recessive and dominant. A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins. A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The SiLM1040/2/4S transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver.

TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant time out. The receiver remains active and biased to VCC/2 and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

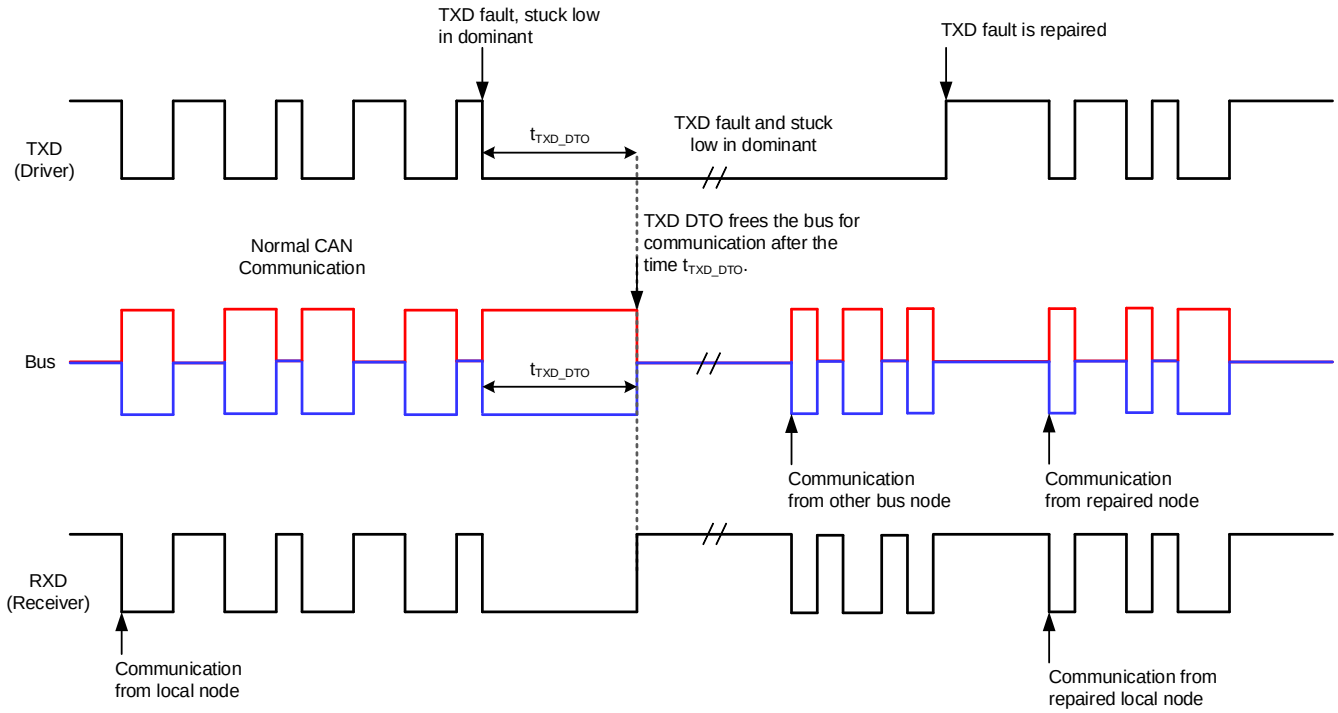


Figure 13. Example of timing diagram for TXD DTO

Under-Voltage Lockout

The SiLM104x/5xS integrates under-voltage detection. It protects the bus during an under-voltage event on either the VCC or VIO supply.

Table 1. Under Voltage for VCC only device

VCC	Device State	Bus Output	RXD
>UVLO	Normal	Depends on TXD	Mirrors Bus[1]
<UVLO	Protected	High Impedance	High Impedance

1) Mirrors bus: low if CAN bus is dominant; high if CAN bus is recessive.

Table 2. Under Voltage for VCC and VIO device

VCC	VIO	Device State	Bus Output	RXD
>UVLO	>UVLO	Normal	Depends on TXD	Mirrors Bus
<UVLO	>UVLO	STB=High: Standby Mode	Recessive	Bus Wake RXD Request
		S=High: Silent Mode	Recessive	Mirrors Bus
		STB=Low: Protected Mode	High Impedance	High (Recessive)
		S=Low: Protected Mode	High Impedance	High (Recessive)
>UVLO	<UVLO	Protected	High Impedance	High Impedance
<UVLO	<UVLO	Protected	High Impedance	High Impedance

Unpowered Device

The device is designed to be an ideal passive or no load to the CAN bus if the device is unpowered.

The bus pins were designed to have low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

Floating Terminals

The SiLM104x/5xS has internal pull up circuit on the TXD, STB/S pins to put the device in a known state if these pins are floating. The TXD pin is pulled up to VCC or VIO to force a recessive input when it is open. The STB/S pin is pulled up to VCC or VIO to force the device into standby mode or silent mode.

Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

Standby Mode

This is the low power mode of the SiLM1040/2/4S. The CAN driver and main receiver are switched off and bidirectional CAN communication is not possible. The low power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. The local CAN protocol controller should monitor RXD for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB pin low. The CAN bus pins are weakly pulled to GND in this mode. In standby mode of SiLM1040S, only the VIO supply is required therefore the VCC voltage may be switched off for additional system level current savings.

Silent Mode

This is the silent mode of the SiLM1050/1/7S. In silent mode the CAN driver is disabled and the high-speed CAN receiver is enabled. CAN communication is unidirectional into the device where the receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The SiLM1040/2/4S supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation by a falling edge and low corresponding to a filtered dominant on the RXD.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. These filtered dominant, recessive, dominant pulses do not need to occur in immediate succession. Once the first filtered dominant signal is received, the device is now waiting for a filtered recessive signal, other bus traffic will not reset the bus monitor. Once the filtered recessive signal is received, the monitor is now waiting for a second filtered dominant signal, and again other bus traffic will not reset the monitor.

Once a full WUP has been detected, the device will transition to driving the RXD output pin low for the remainder of any dominant signal that remains on the bus for longer than t_{WK_FILTER}.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value, $t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in its current state without waking up.

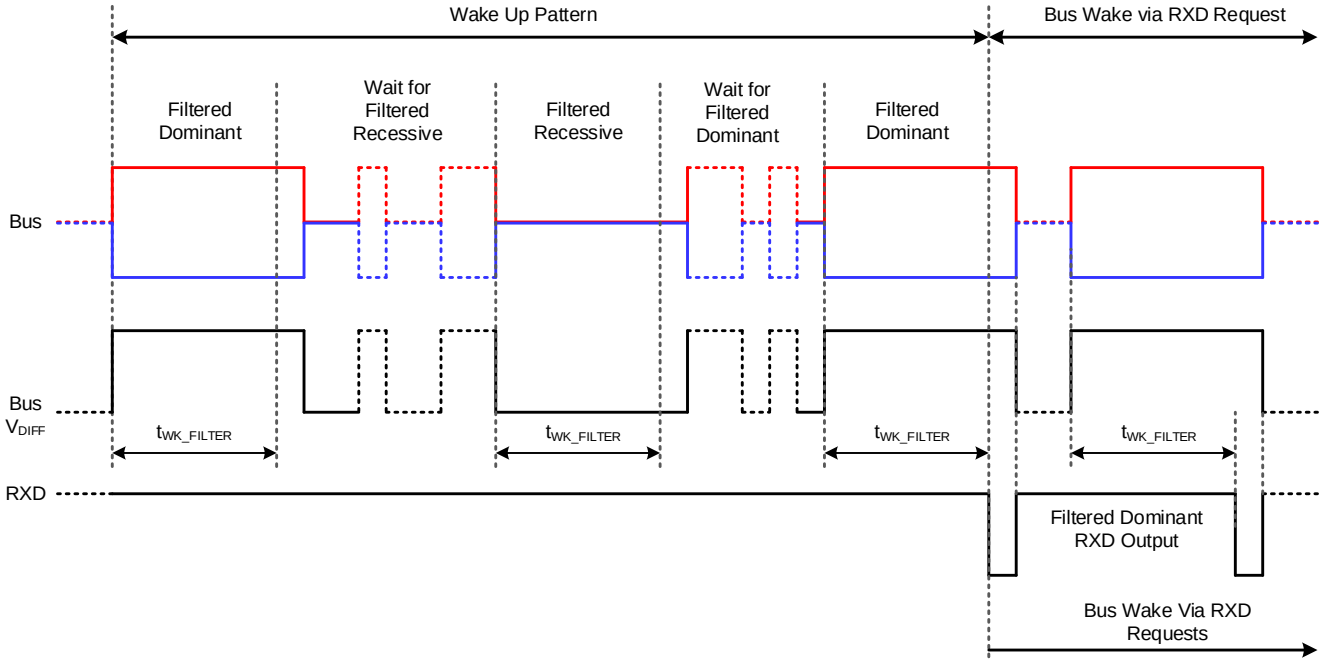
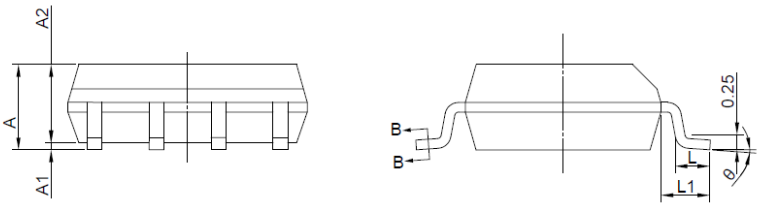


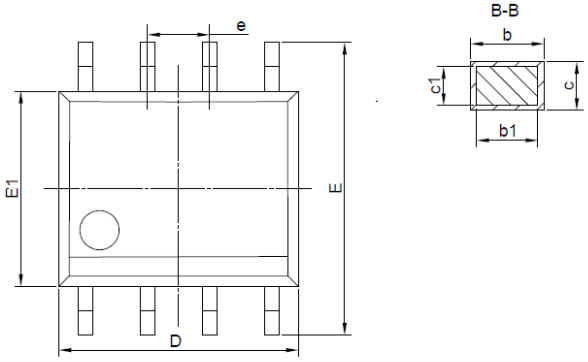
Figure 14. Wake up pattern (WUP)

Thermal Shutdown

The SiLM104x/5xS integrates the thermal shutdown protection. If the junction temperature exceeds the thermal shutdown threshold, the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver to RXD path remains operational. A 15°C hysteresis is included so that the SiLM104x/5xS does not recover from thermal shutdown until the on-chip temperature drops below 175°C.

PACKAGE CASE OUTLINES





Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	4.7	4.9	5.1
E	5.8	6	6.2
E1	3.8	3.9	4
e	1.02	1.27	1.52
Unit : mm			

Figure 15. SOP8 Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: 2023-09-11	
Whole document	Initial datasheet release